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AESO PSSE Dynamic Model Performance Test Bench Guideline

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Classification: Public

Tool Revision History

Revision	Description of Revision	Date
V1	Initial Release	April 9, 2025
V2	<ul style="list-style-type: none"> • Added option to modify generator voltage setpoints in the Basic Simulation Setup • Added option to include load channels in the monitored channel list to better support composite load projects • Added option to scale voltage playback profiles by regional nominal voltages to accommodate increased POC controls in IBRs across different areas. • Added support for reading sequence files • Added support for incorporating DLL libraries • Added single-phase fault recovery tests • Added reference step tests for PLNTBU models in addition to REPC models • Improved Point of Connection identification routine for broader facility model compatibility • Updated default step size for the Frequency Reference Step Change test from 0.05 to 0.005 • Updated equivalent impedance calculation in the Short Circuit Ratio Test to define P as the sum of all generator P_{max} values at the facility • Updated HVRT voltage profile to align with ISO requirements • Updated zero-impedance line reactance from 0.0001 to 0.00012 to improve numerical stability in PSSE • Basic simulation setup is now divided into System and Facility, letting users modify the facility setup without impacting system settings, including infinite bus voltage and interconnection line impedance. • Instructions for completing the sheet have been updated for clarity and conciseness. • Various bug fixes and performance enhancements. 	February 4, 2026

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1. Background

The AESO PSS®E Dynamic Model Performance Test Bench is a tool developed by the Alberta Electric System Operator (AESO) to assist internal and external stakeholders in evaluating the performance of PSS®E dynamic models under various conditions and identifying potential modeling issues. This document provides guidance on case preparation and the effective use of the Test Bench.

2. Applicability

This Test Bench applies to all generation facilities and industrial complexes with generators at both transmission and distribution levels, including synchronous generators and inverter-based generators such as wind, solar and battery storage.

The test requirements are contained in the PDUP Checklist. Related references should be reviewed if applicable to the facility under study, which could include:

- AESO Connection Requirements for Inverter-Based Resources (February 2024)
- ID# 2010-001R Facility Modelling Data and List of Electrical and Physical Parameters for Transmission System Model
- ID# 2017-013R Model Validation and Reactive Power Reporting Guidance
- Section 503.4 Voltage Regulation
- Section 503.5 Voltage Ride Through
- Section 503.6 Frequency and Speed Governing
- AESO DER Roadmap Integration Paper - DER Ride-Through Performance Recommendations

3. Acronym

BESS - Battery energy storage system

DER - Distributed energy resource

IBRs - Inverter-based resources

OPBC - Operational Planning Base case

PBCS - Planning Base Case Suite

POC - Point of connection

SMIB - single machine infinite bus system

4. Running the Test Bench

4.1 Test Bench Prerequisites

The Model Performance Test Bench is an executable file (.exe) designed for use with PSS®E software. It is compatible with PSS®E versions 35 and 36.

The release includes:

- Model Performance Test Bench (for PSS®E version 35, 36)
- InputSheet (.xlsx)
- PSS®E Dynamic Model Performance Test Bench Guideline

4.2 Preparing the Power flow base case

This Test Bench facilitates the evaluation of dynamic model performance using the isolated Single Machine Infinite Bus (SMIB) system.

The power flow cases shall be prepared as follow:

The test generation shall be modeled in the power flow case as follows: A slack bus with an infinite machine (large Mbase = 9999 MVA and small $X_{source} = 0.01$ pu) is connected to the generation facility via a zero-impedance tie line ($X = 0.00012$ pu). The SMIB connections for different connection types and generation technologies are detailed below.

- For Inverter-based resources (IBRs) to comply with the "AESO Connection Requirements for Inverter-Based Resources", the SMIB system shall be connected to the Interconnection line of the generation facility, which connects to either a T-tap or a substation, depending on the configuration. The impedance of the interconnection line should be included based on the project's design specifications. If these specifications are unavailable, reasonable assumptions should be made to ensure accurate modeling.

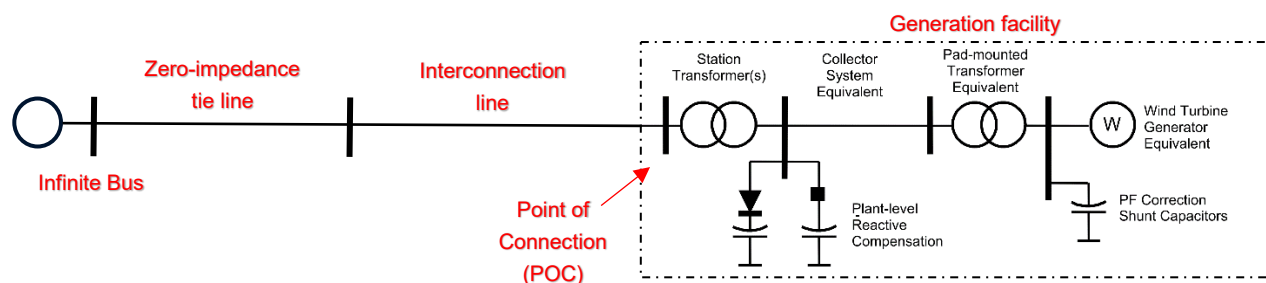


Figure 1 Network Diagram for IBRs comply with IBR connection requirement

- For Conventional machines or IBRs which are not required to comply with the “AESO Connection Requirements for Inverter-Based Resources”, the SMIB system shall be connected to the POC of the generation facility.

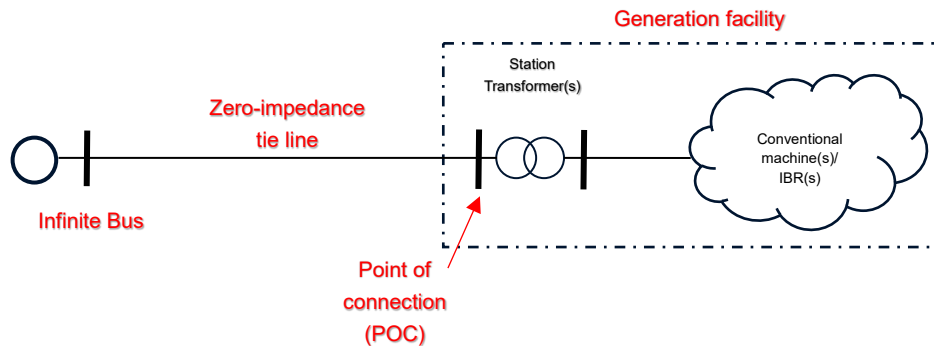


Figure 2 Network Diagram for conventional machine or IBRs not comply with IBR connection requirement

- For Distributed Energy Resources (DER) of any technology, the SMIB system shall be connected to the high voltage side of the grid-connected substation transformer. Detailed information for the substation transformer can be obtained from the Planning Base Case Suite (PBCS) or Operational Planning Base case (OPBC) which can be provided by the AESO on request.

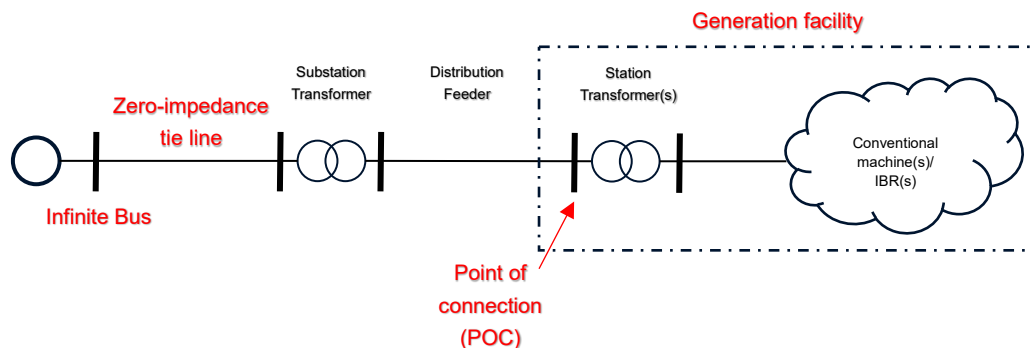


Figure 3 Network Diagram for DER

The DYR file of the test generation facility should align with the power flow case, with the following notes:

- Generator bus number and ID must match those in the power flow case.
- Model selection must correspond to the generator type/ technology based on the latest WECC approved model list (can be found on the WECC website), unless otherwise approved by AESO.
- A dynamic model of the infinite machine is not required.
- User-defined models are now supported.

4.3 Running the Test Bench

In the **InputSheet.xlsx** file, users can define input files, configure basic simulation settings, specify test cases, and select export formats directly within an.xlsx file. Each field is accompanied by detailed instructions to ensure easy and efficient completion.

4.3.1 Input files

In the *Input* section, users can define project details and specify input file locations. The Test Bench is designed to accept the following PSS@E file types, representing either the complete model with SMIB system or up to the Point of Connection (POC), as listed in Figure 4:

- Power Flow Data Files (.raw)
- Saved Case Files (.sav)
- Response Files (.idv)

INPUT FILES	This section enables the specification of the required file locations	
Project No.	Enter the 4 digit project #####	1234
Stage No.	Enter the 1 digit stage #	0
File Path	The complete path to the directory containing your input files	C:\myproject
Output Folder	The name of the output folder for storing simulation results, located within the specified <i>File Path</i>	DYR_RESULTS
Facility Model	Accept any of the following file types: .idv, .raw, .sav of the complete test model or up to the Point of Connection (POC).	myproject.sav
SEQ Model	Accept : .seq.idv, .seq (optional; required only for single-phase fault recovery tests)	myproject.seq.idv
DYR Model	Accept : .dyr	myproject.dyr
Model Library(ies)	Accept : .dll files (;-separated; include all dependencies within the specified <i>File Path</i>)	myproject_1.dll;myproject_2.dll

Figure 4 Input file section

4.3.2 Simulation setup

In the *Simulation Setup* section, the user shall specify the simulation parameters as shown in Figure 5. This includes:

- **Simulation time step (DELTA):** Set to $\frac{1}{4}$ cycle by default.
- **System transformer high-voltage side voltage range:** By default, configured between 69 kV and 500 kV to assist the tool in identifying the point of connection for the generating facility.
- **Monitored Channels:** Set to 1 to include additional Pload and Qload Channels.
- **Interconnection Line Impedance:** In the simulation setup for inverter-based resources (IBRs), there is an option to include the interconnection line when creating the base case. By setting this field to any value greater than 0, the interconnection line is incorporated into the model if the generating facility is represented up to the Point of Connection (POC). For conventional machines or DERs, set this value to 0. Do not leave it empty as it will trigger an error.
- **System Equivalent Reactance:** For fault recovery and reference setpoint step tests, the zero-impedance tie line reactance should be replaced with the System Thevenin equivalent reactance. This equivalent can be determined using the latest PBCS or OPBC with the generation facility modeled. If this information is unavailable, reasonable assumptions should be made to ensure accurate modeling.
- **Infinite Bus Voltage:** Represents the system's normal operating voltage in per unit
- **Generation Active Power Output:** Specified in per unit (pu), ranging between 0 and 1.
- **Battery Energy Storage System (BESS) Active Power Output:** Defined in per unit (pu), with negative values indicating charging mode and positive values indicating discharging mode.
- **Motor Active Power Consumption:** defined in per unit (pu) with negative values.

BASIC SIMULATION SETUP		
Simulation Time Step	Simulation time step in seconds	0.0041667
Simulation Duration	Minimum simulation duration in seconds	20
Monitored Channels	Set to 0 to include only default channels (bus pu voltage, frequency deviation, machine P, Q, and rotor angle). Set to 1 to also include Pload and Qload; recommended for load projects.	0
Transmission Voltage Level Lower Bound	Used to identify the POC, defined as the main power transformer high side . Specify the lower bound in kV.	69
Transmission Voltage Level Upper Bound	Used to identify the POC, defined as the main power transformer high side . Specify the higher bound in kV.	500
Insert SMIB?	Set to 1 to insert an SMIB through a zero-impedance tie line to the most upstream bus provided. An optional tap bus can be added in between via the "Interconnection Line Reactance" field. This function supports only a single POC; for multiple upstream buses, build the full test case manually. (default infinite bus number = 9999, voltage = 1.0 p.u.).	0
Interconnection Line Reactance	Enter the line reactance between the POC and the POI (i.e., the transmission system tap point). Use 0 if no line is required (common for conventional machines or DERs). For IBRs, if the exact impedance is unavailable, a default value of 0.01 may be used. This field is ignored when "Insert SMIB?" is disabled, since a full test case is assumed to be provided. (default tap bus number = 999, voltage = 1.0 p.u.).	0
System Equivalent Reactance	This value is used in the <i>Fault Recovery (FR)</i> and <i>Reference Step Change (RSC)</i> tests as the equivalent reactance that replaces the <i>zero-impedance tie line</i> connecting the facility to the SMIB. Determine this using the latest OPBC case. If unavailable, approximate using SCR = 3 for IBRs or SCR = 5 for conventional generators: $X_{pu} = 1 / (SCR \times P_{pu})$ where P_{pu} is the plant's maximum active power at the POC on a initial voltage of the infinite bus. All <i>Voltage (p.u.)</i> values in subsequent test tabs are scaled by this value.	0.01
Inf Bus Voltage	Set to the service-area nominal voltage in p.u., calculated using the PSSE voltage bases (69, 138, 240, 500 kV). e.g., 138/138 = 1.0, 144/138 = 1.043 Set to ≤ 0 to leave the voltage unchanged when a full test case is loaded.	1.043
Enable Setup	Set this value to 1 to apply the settings below, or 0 to keep existing test case settings.	1
GEN P%	Initial Pgen as a percentage of Pmax (+) A machine with Pmin ≥ 0 is treated as a regular GEN	1
BESS P%	Initial Pgen as a percentage of the Pmax (+), Pmin (-) A machine with Pmin < 0 and Pmax > 0 is treated as a BESS	1
MOTOR P%	Initial Pgen as a percentage of Pmin (-) A machine with Pmin < 0 and Pmax = 0 is treated as a Motor	1
Gen Voltage Setpoint	Generator voltage setpoints. Set to ≤ 0 to leave the voltages unchanged from the facility model.	1

Figure 5 Simulation setup section

4.3.3 Specify AESO dynamic model performance tests

The *Tests* section outlines the model performance evaluations detailed in Table 1 and Figure 6.

For voltage (VOLT) and frequency (FREQ) tests, the PLBVFU1 model is used at the infinite machine to play back voltage and frequency signals defined in the respective sheets of the InputSheet.xlsx file. Each sheet is named after the corresponding test listed in the *Test* section. For voltage and frequency ride-through test, please refer to the PDUP Checklist for requirements specific to the generation type.

For Fault recovery test (FR) and Reference setpoint step test (RSC), the system equivalent reactance needs to be specified as per section 4.3.2.

Notation	Test Type
FS	Flat start
VOLT	Voltage response tests (Voltage step up and down, voltage ride through)
FREQ	Frequency response tests (Frequency step up and down, frequency ride through)

FR	Fault recovery test
SCR	Short-circuit ratio test – Intended for transmission connected IBRs
RSC	Reference setpoint step test (Voltage reference, Frequency reference) – Intended for transmission connected IBRs.

Table 1 Performance test type

TESTS	Enter '1' for each test below that needs to be run. Test codes are described below: Flat Start Test (FS) Voltage and Frequency Playback Tests (FREQ, VOLT): The voltage and frequency profile tabs (in this workbook), are pre-assigned and may be edited if needed. Each tab must include the following column titles: Time (sec), Voltage (p.u.), Frequency (Hz) Add additional playback tests by inserting rows within this TESTS section Fault Recovery (FR) Tests: Enter the fault type ("1-phase" or "3-phase") and the fault duration in seconds within square brackets. Note that sequence data is required to properly run a single-phase fault. Short Circuit Ratio (SCR) Tests: Enter the SCR values within square brackets, followed by the fault duration in seconds. (Applies to IBRs only) Reference Step Change (RSC) Tests: Enter the reference type ("VOLT-RSC", or "FREQ-RSC") in quotations and the step change percentage within square brackets. (Applies to IBRs with the REPCA model or the PLNTBU1 model)	
FS	FS	1
FREQ	FRQ-STEP-UP	
FREQ	FRQ-STEP-DOWN	
VOLT	VLT-STEP-UP	1
VOLT	VLT-STEP-DOWN	1
VOLT	HVRT	
VOLT	LVRT	
FREQ	HFRT	
FREQ	LFRT	
VOLT	HVRT-IBR	1
VOLT	LVRT-IBR	1
FREQ	HFRT-IBR	
FREQ	LFRT-IBR	
FR	['1-phase', 0.1]	1
FR	['3-phase', 0.1]	1
SCR	[8,5,3,2,1.9,1.7,1.5,1.3], 0.1	1
RSC	['VOLT-RSC', 0.05]	1
RSC	['FREQ-RSC', 0.005]	

Figure 6 Performance test section

4.3.4 Specify output file format

Simulation outputs are saved in .sav and .pdf formats. Additionally, the *Export* section allows for the inclusion of .csv and .svg output formats, as shown in Figure 7.

EXPORT	The following files will be automatically saved: the test case in .raw or .sav, result plots in a .pdf file, and simulation data in .out format. Additionally, you have the option to save the data in .csv format.	
.csv	dynamic simulation results	1
image	dynamic simulation result plots	1

Figure 7 Export section

4.3.5 Run tests

To execute the Dynamic model performance tests:

1. Enable the Run: Set “Run Status” to 1 to enable the simulation run, as illustrated in Figure 8. If set to 0, model performance tests will not run. If multiple scenarios are being utilized for the project and the same tests need to be run, assign a unique name to each output folder to differentiate simulation results.
2. Launch the Executable: Open the AESO_MPTB.exe file for your specific PSS®E version.
3. Select PSS®E Version: Within the application, choose the appropriate PSS®E version from the available options.
4. Load Input File: Click on "Browse Input File" and navigate to select the InputSheet.xlsx file containing your test configurations.

INPUTS	NOTES		
Run Status	Set to 0 to disable a round while preserving setting records	1	0
INPUT FILES	This section enables the specification of the required file locations		
Project No.	Enter the 4 digit project #####	1234	1234
Stage No.	Enter the 1 digit stage #	0	0

Figure 8 Run Status to enable simulation run

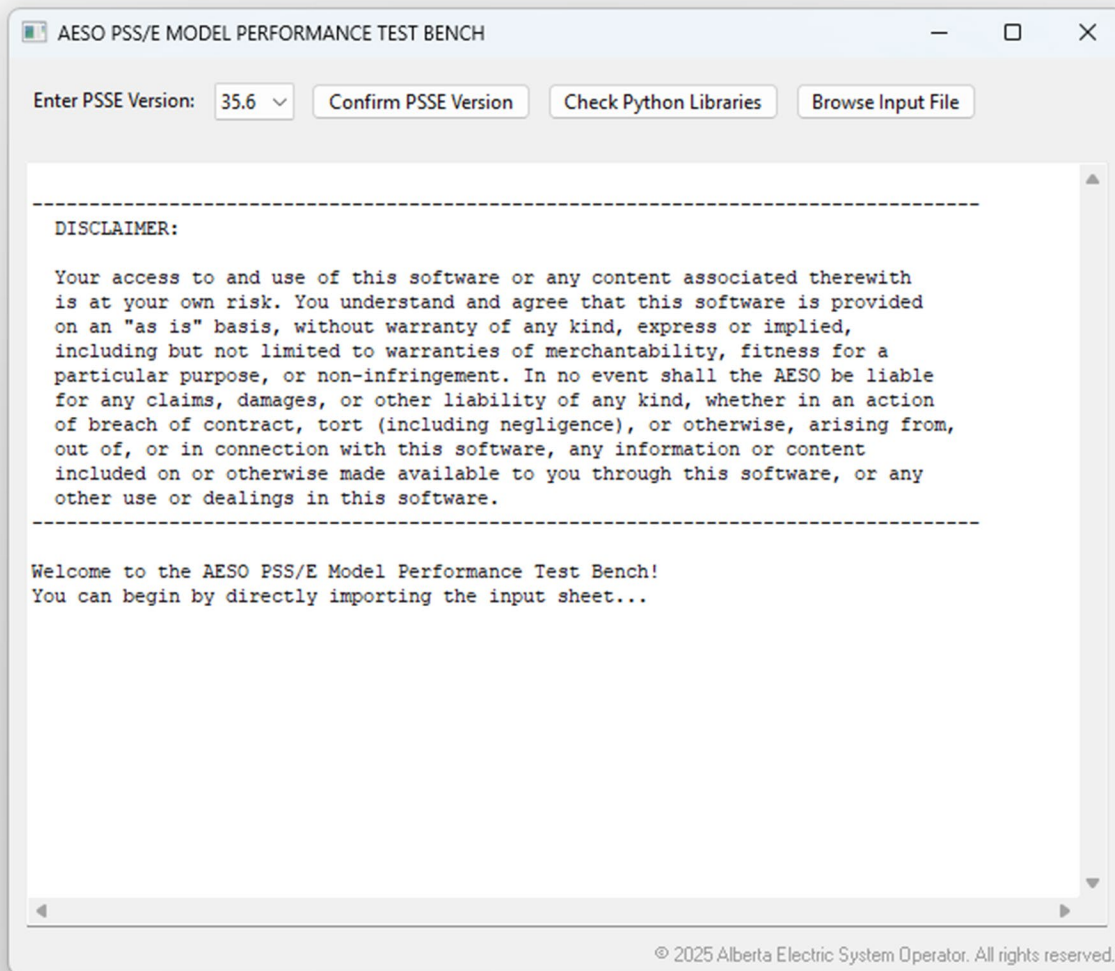


Figure 9 Model Performance Test Bench

4.4 Output files

The *Results* folder is created within the directory specified in the *Input* section, as illustrated in Figure 10. This folder contains subdirectories named according to each test type, which include the following output files:

- test case (.raw)
- converted case (.sav)
- snap file (.snp)
- PSS/E log file
- outfile (.out)
- result pdf (.pdf)
- output file (.csv) – optional
- result image (.svg)

Additionally, the program's run-time log files can be found in the *AESO_MPTB_RUN_LOG* folder, located in the same directory as the .exe file.

Name	Type
FRQ-STEP-UP	File folder
FS	File folder
VLT-STEP-UP	File folder
COMBINED RESULTS_FS_FRQ-STEP-UP_VLT-STEP-UP	Adobe Acrobat Document
myproject	RAW File
myproject	DYR File

Figure 10 Result folder structure

The following signals will be monitored in the simulations and saved in the output file. These monitored signals are essential for analyzing the dynamic performance and stability of the power system during various operating conditions and disturbances.

- **Active power:** The real power output of the test generators and infinite machine, measured in per unit.
- **Reactive power:** The reactive power output of the test generators and infinite machine, measured in per unit.
- **Bus angle:** The angle magnitude at generator bus, POC and infinite bus, measured in degree
- **Bus voltage:** The voltage magnitude at generator bus, POC and infinite bus, measured in per unit
- **Bus frequency:** The frequency magnitude at generator bus, POC and infinite bus, measured in per unit

The result PDF shall be stamped and sealed by a professional engineer with APEGA and shall be included in the submission of the PUDP and the PUDP Checklist.

5. Additional Information

5.1 Short circuit ratio test

This test will demonstrate IBR facility performance under weak grid conditions given system strength at POC is subject to variation triggered by outages, network reconfiguration, etc. The model shall be tested for a set of short circuit ratios (SCRs) at the POC starting from a strong system condition and moving towards a weaker condition. The SCR adjustment is achieved by varying the reactance of the zero-impedance tie line. The simulation starts at a pre-defined SCR followed by applying a solid three phase to ground fault at the POC which will be cleared after 6 cycles. The SCR will then be changed to a lower value and the fault will be applied again at a time interval of 5 seconds, and so on. The default settings of the SCR input are [5,3,2,1.5,1]. The definition of SCR is:

$$SCR = \frac{SCMVA}{\sum ABS(P_{gi})}$$

$SCMVA$ = short circuit MVA measured at POC

P_{gi} = rated active power output (MW) of the test generator i

Consider an example of a facility comprising wind generation ($P_{gen} = P_{max} = 80$ MW) and a BESS with a maximum discharge power of 20 MW and a minimum charge power of -20 MW, operating with an SCR of 5. The reactance of the zero-impedance tie line is identical for the BESS operating in either charging or discharging mode, and can be calculated as follows:

$$SCMVA_{discharge} = SCR \times \sum ABS(P_{gi}) = 5 \times (80 + |20|) = 500$$

$$line\ reactance_{discharge} = \frac{system\ MVA}{SCMVA} = \frac{100}{500} = 0.2\ pu$$

$$SCMVA_{charge} = SCR \times \sum ABS(P_{gi}) = 5 \times (80 + |-20|) = 500$$

$$line\ reactance_{charge} = \frac{system\ MVA}{SCMVA} = \frac{100}{500} = 0.2\ pu$$

6. Troubleshooting

This section offers a comprehensive overview of common errors encountered while using the tool, along with their respective resolutions. Its primary objective is to assist users in efficiently diagnosing and addressing these issues.

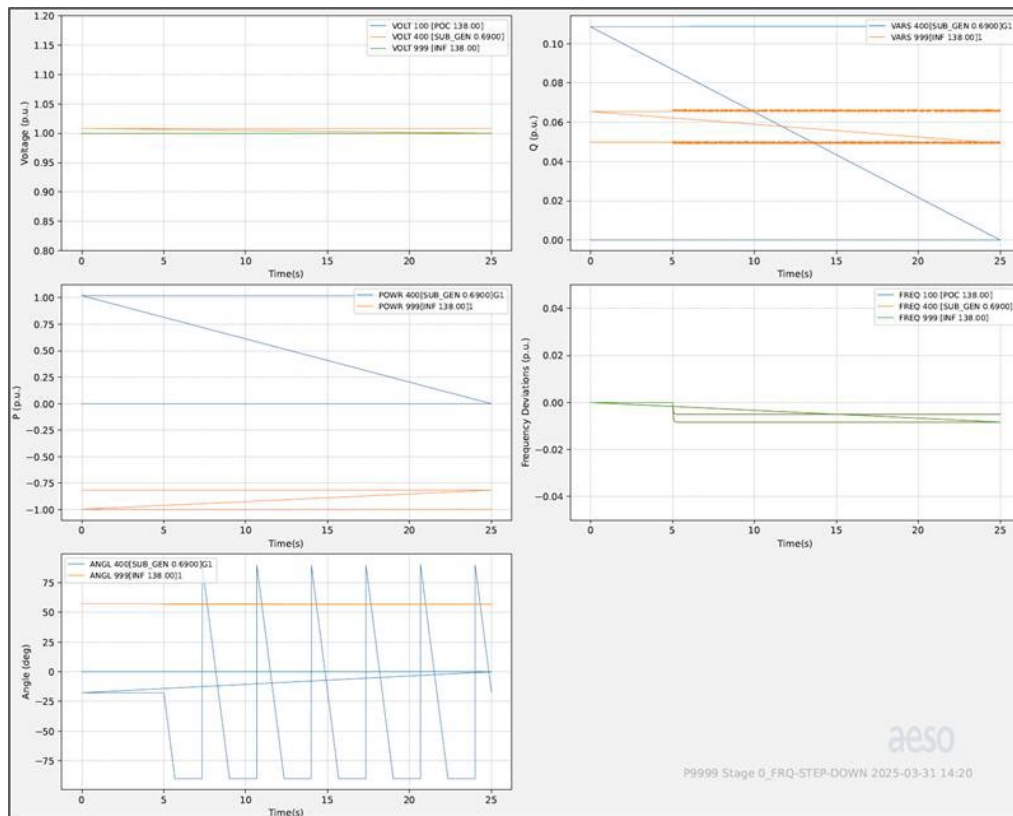


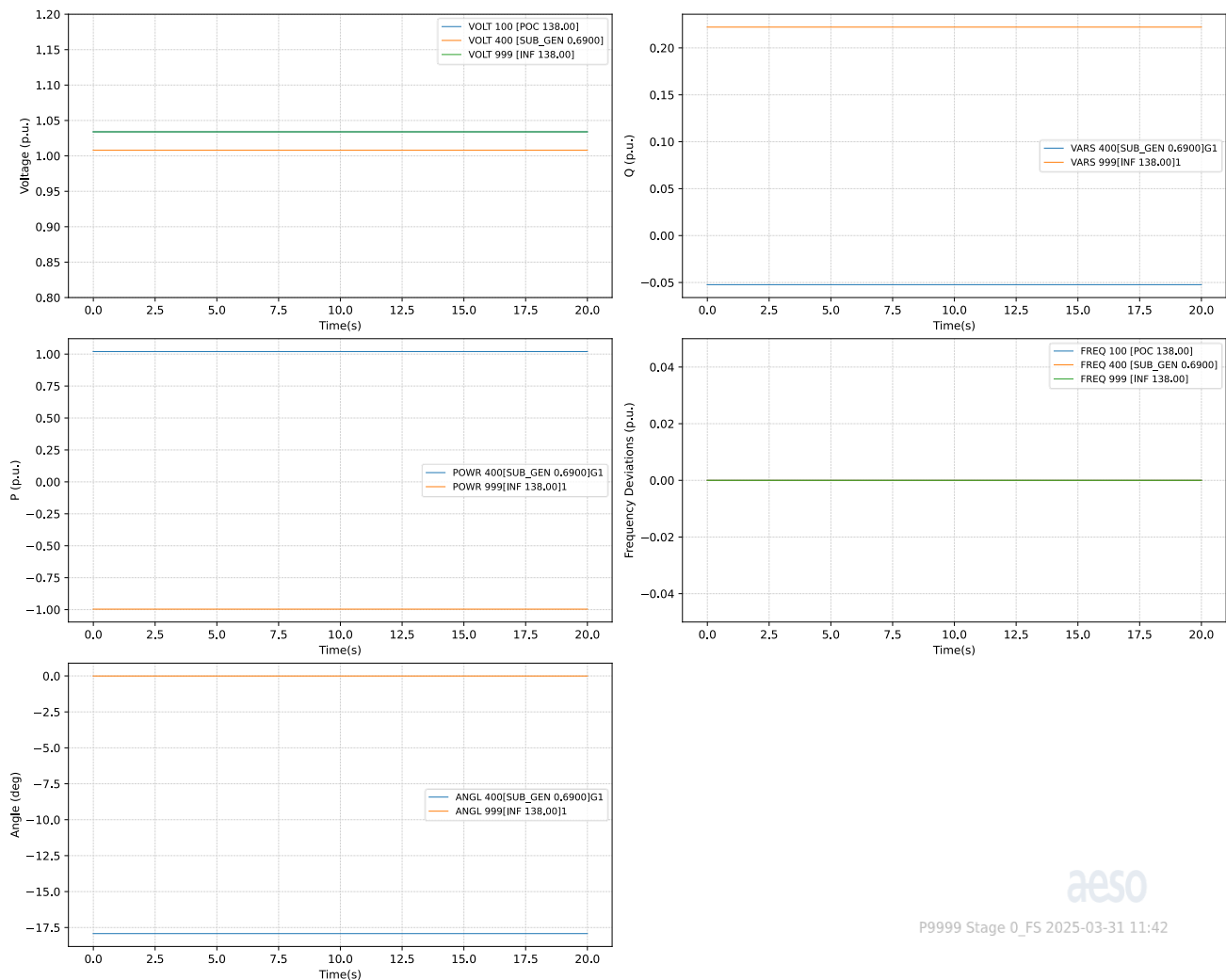
Figure 12 Sample plotting error results

7. Sample Results

Followings are the sample model performance test results of an IBR (wind) facility. For more detail on the test requirements and acceptance criteria correspond to the generation technology, connection type and project stages, please refer to the PDUP Checklist.

7.1 Flat Start

Flat start test showing steady generator voltage, real and reactive power flow.

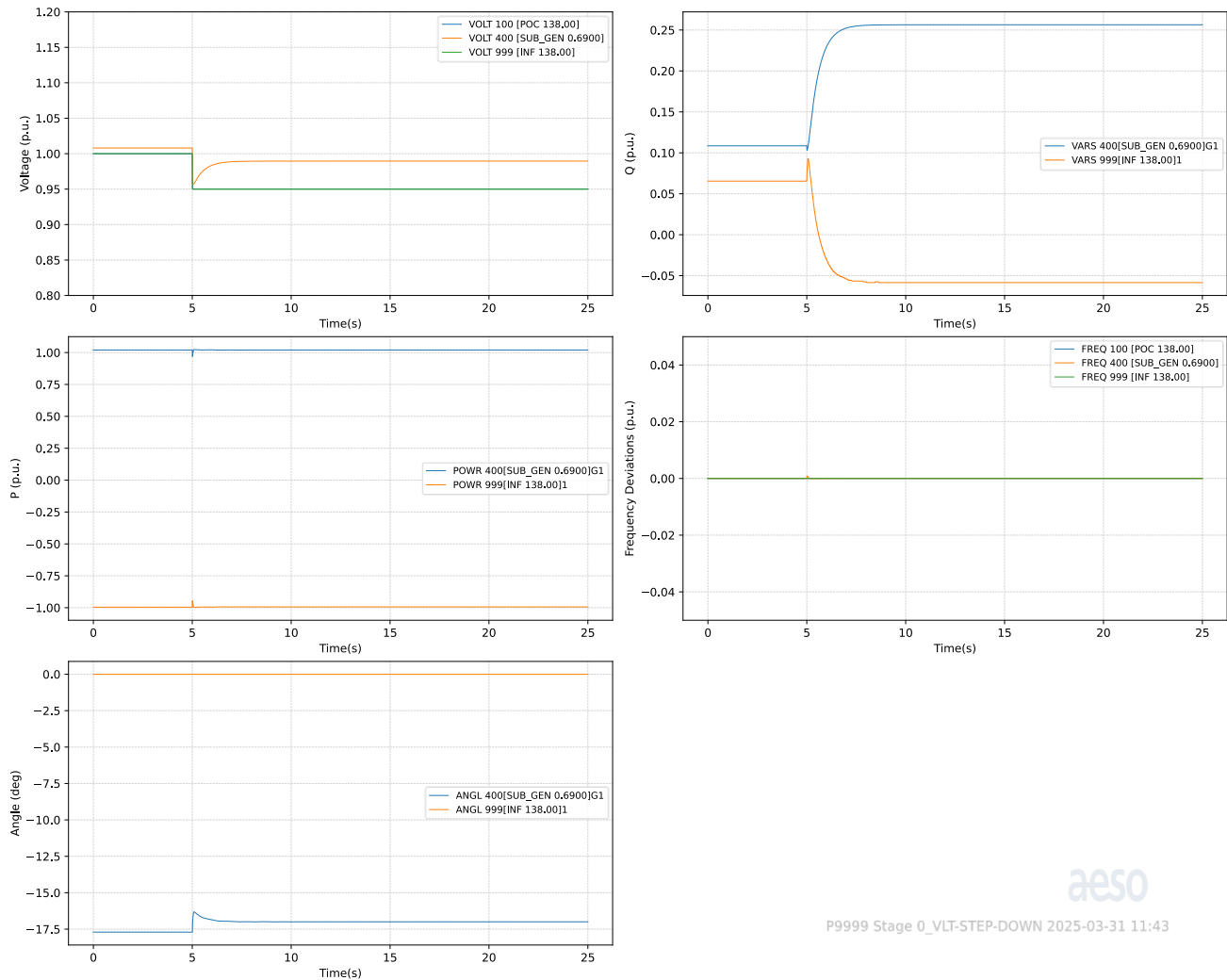


aeso
P9999 Stage 0_FS 2025-03-31 11:42

Figure 13 Sample flat start test result

7.2 Voltage step-down test

Under a 5% voltage step down at the POC, the generator increased reactive power output and maintained real power.

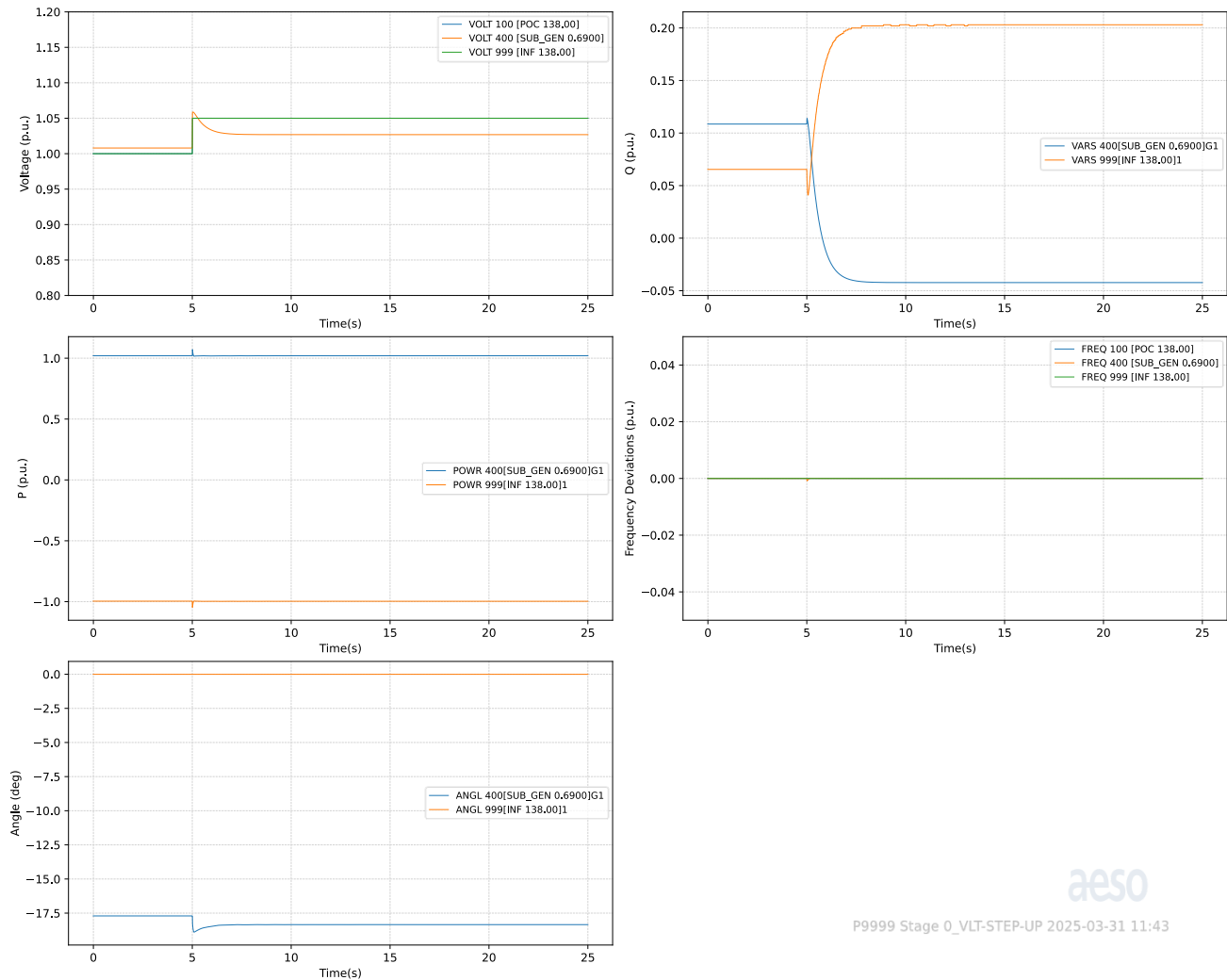


aeso
P9999 Stage 0_VLT-STEP-DOWN 2025-03-31 11:43

Figure 14 Sample voltage step down test result

7.3 Voltage step-up test

Under a 5% voltage step up at the POC, the generator decreased reactive power output and maintained real power.

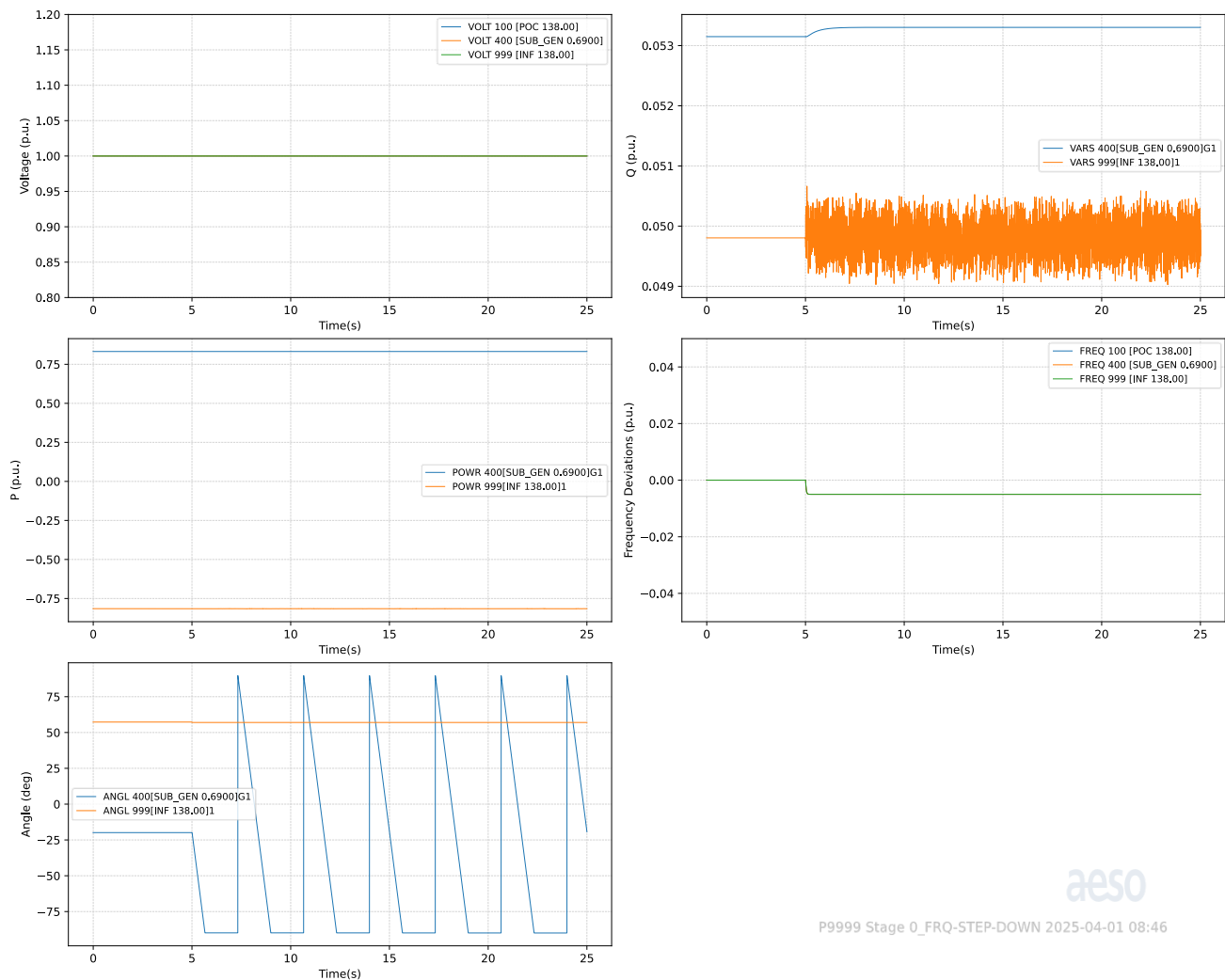


aeso
P9999 Stage 0_VLT-STEP-UP 2025-03-31 11:43

Figure 15 Sample voltage step up test result

7.4 Frequency step-down test

In this test, real power is initialized at 80% of Pmax assumed in the power flow model. For a 0.5% (0.3Hz) decrease in frequency, real power is maintained assuming there is no headroom to increase real power.

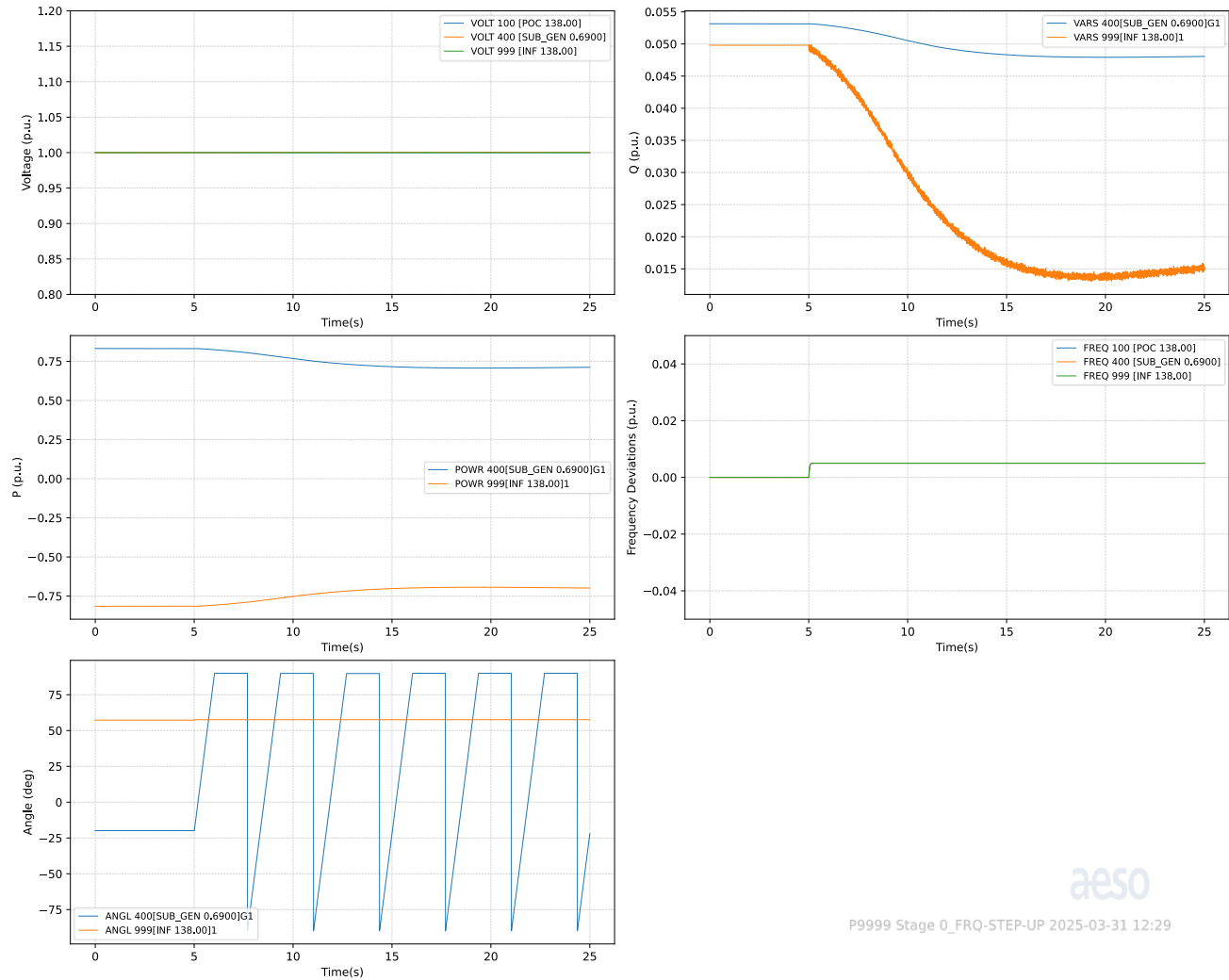


aeso
P9999 Stage 0_FRQ-STEP-DOWN 2025-04-01 08:46

Figure 16 Sample frequency step-down test result

7.5 Frequency step-up test

In this test, real power is initialized at 80% of Pmax assumed in the power flow model. For a 0.5% (0.3Hz) increase in frequency, real power output of the generator decreased.

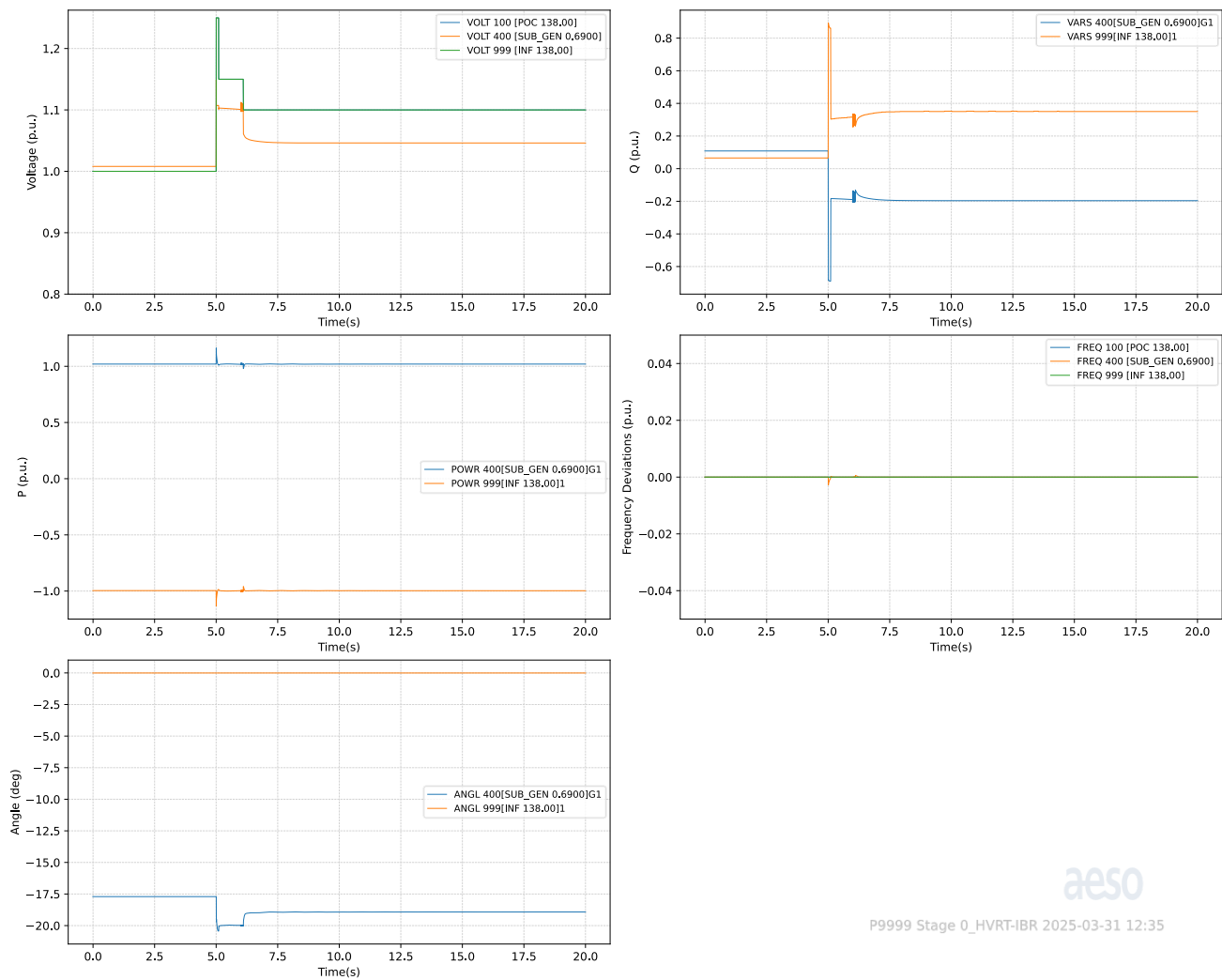


aeso
P9999 Stage 0_FRQ-STEP-UP 2025-03-31 12:29

Figure 17 Sample frequency step-up test result

7.6 High voltage ride-through (HVRT) test

Under the variations of voltages under HVRT specified in the IBR connection requirement, the real power is maintained, and the reactive power absorption decreases in response to the high voltage transient.

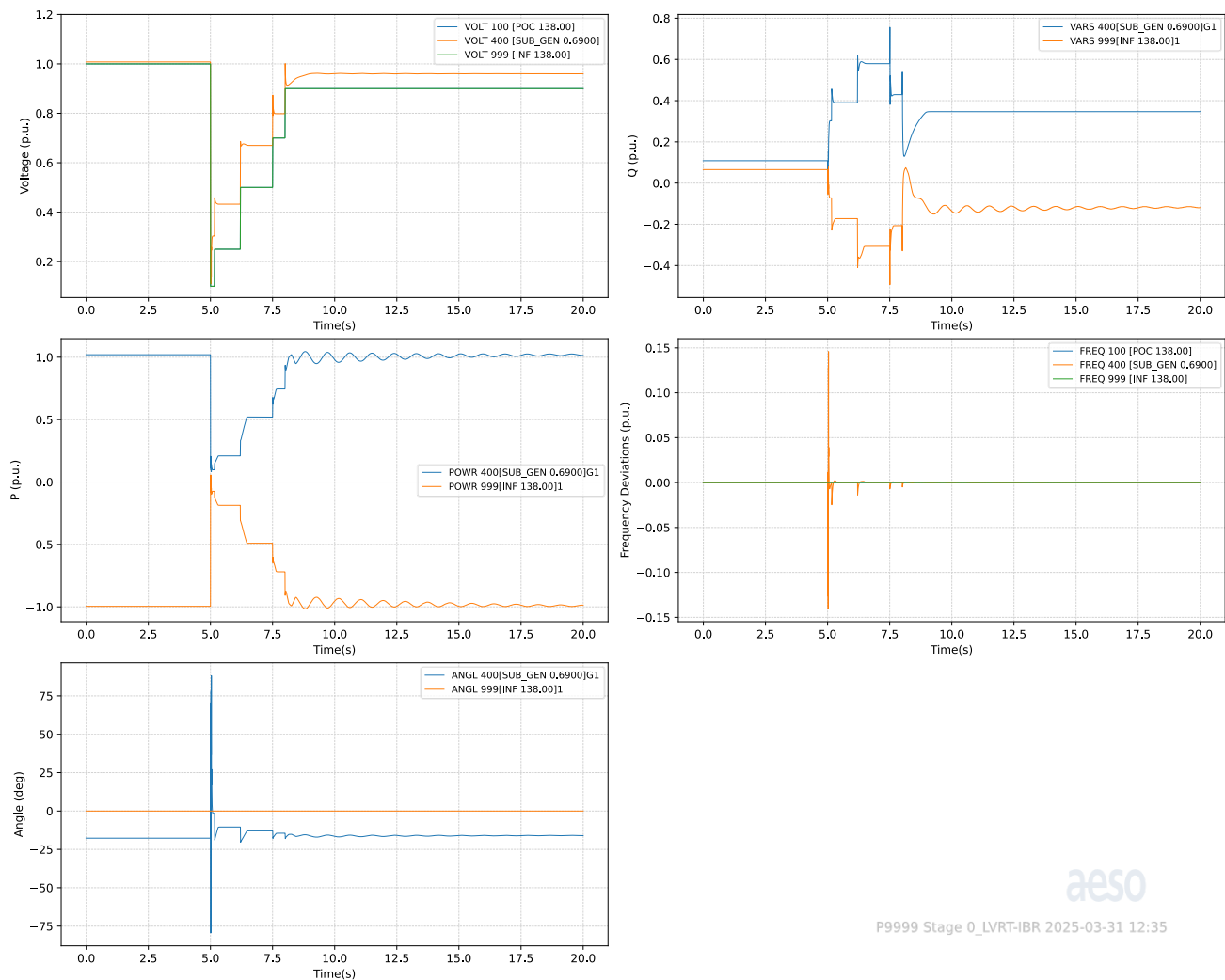


aeso
P9999 Stage 0_HVRT-IBR 2025-03-31 12:35

Figure 18 Sample HVRT test result

7.7 Low voltage ride-through (LVRT) test

Under the variations of voltages under LVRT specified in the IBR connection requirement, reactive power absorption increases in response to the high voltage transient. Active power recovery is acceptable.

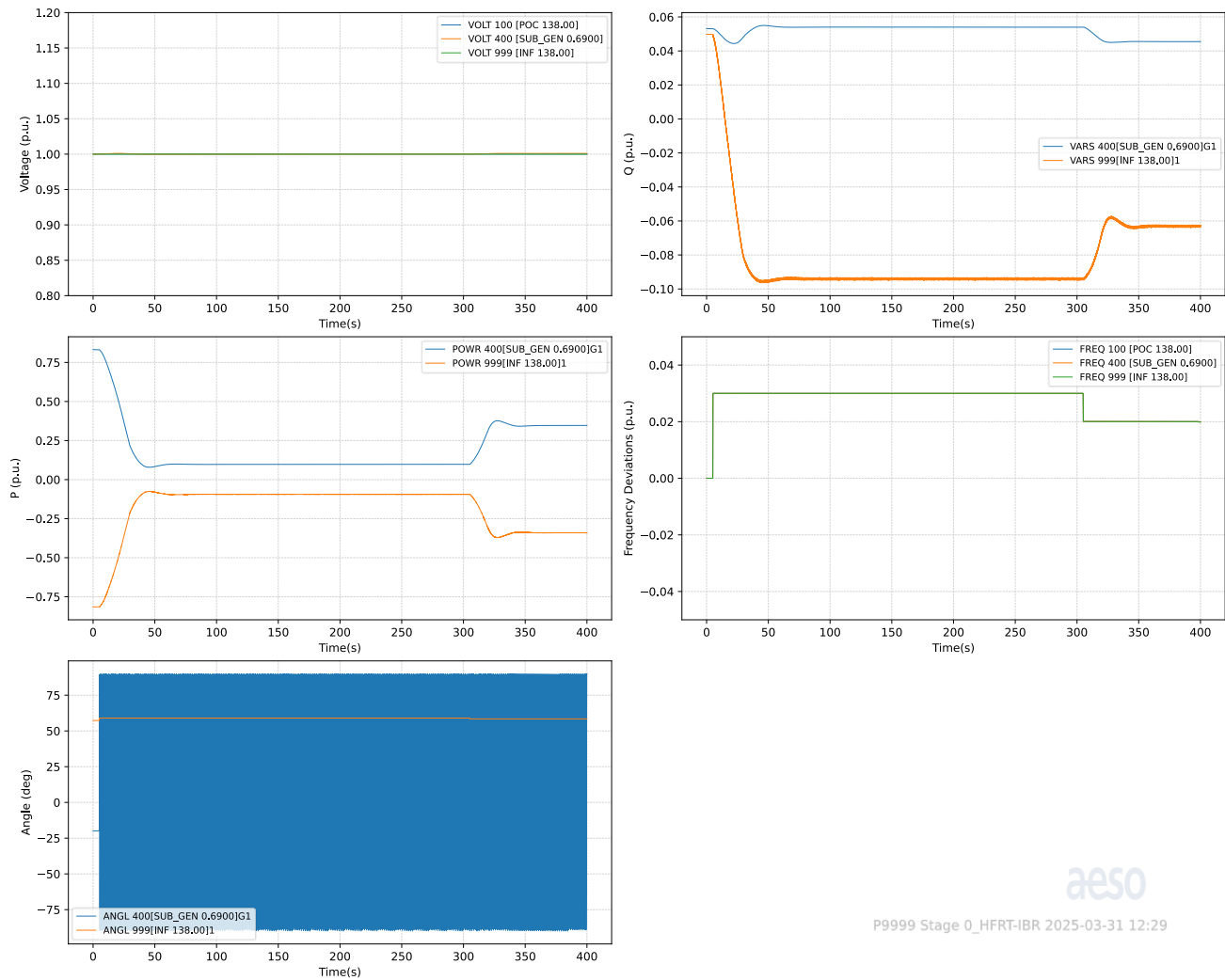


aeso
P9999 Stage 0_LVRT-IBR 2025-03-31 12:35

Figure 19 Sample LVRT test result

7.8 High frequency ride-through (HFRT) test

In this test, real power is initialized at 80% of Pmax assumed in the power flow model. Under the variations of voltages under HFRT specified in the IBR connection requirement, the real power output decreased according to the frequency variation.

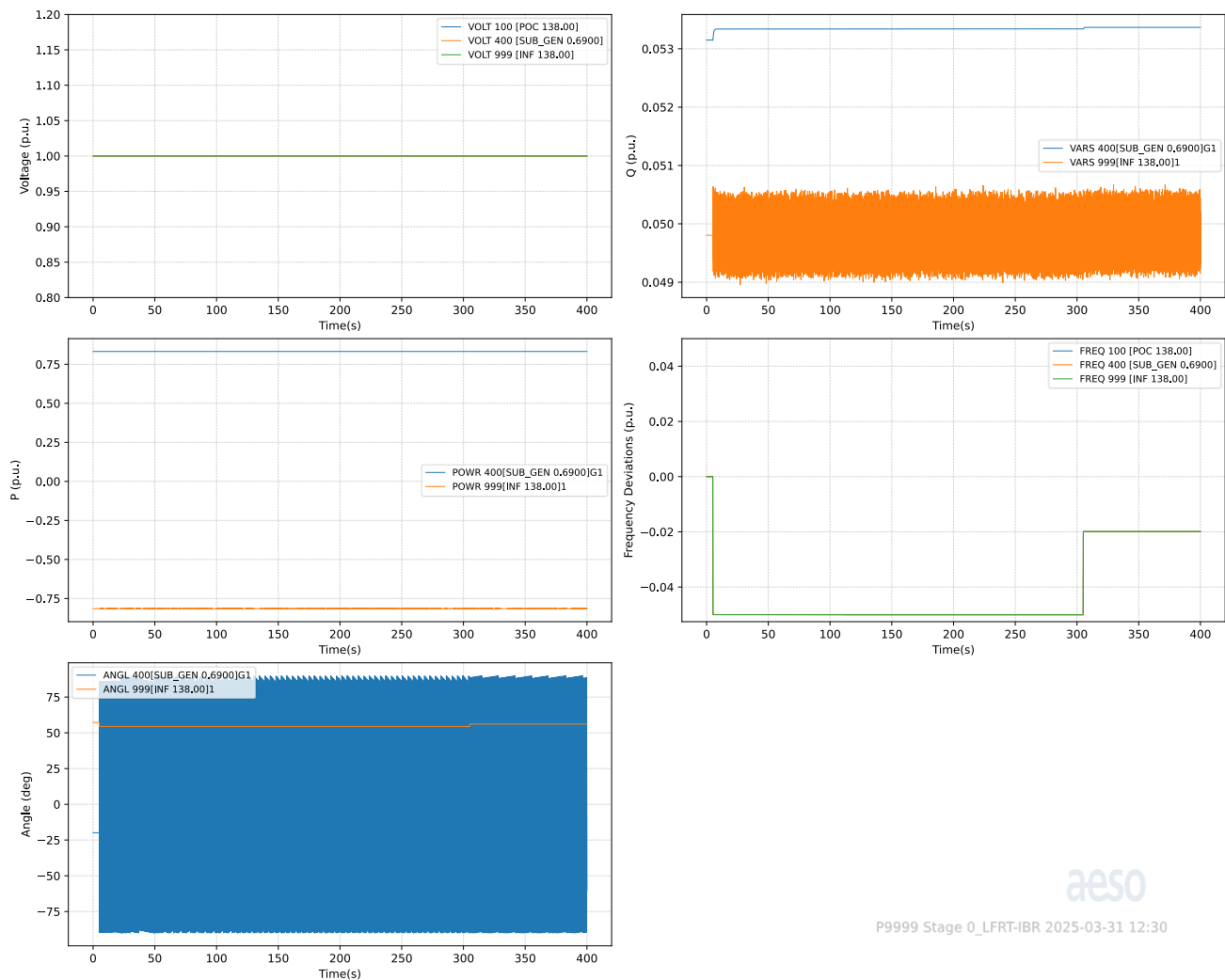


aeso
P9999 Stage 0_HFRT-IBR 2025-03-31 12:29

Figure 20 Sample HFRT test result

7.9 Low frequency ride-through (LFRT) test

In this test, real power is initialized at 80% of Pmax assumed in the power flow model. Under the variations of voltages under LFRT specified in the IBR connection requirement, the real power output remained constant assuming no headroom is reserved.

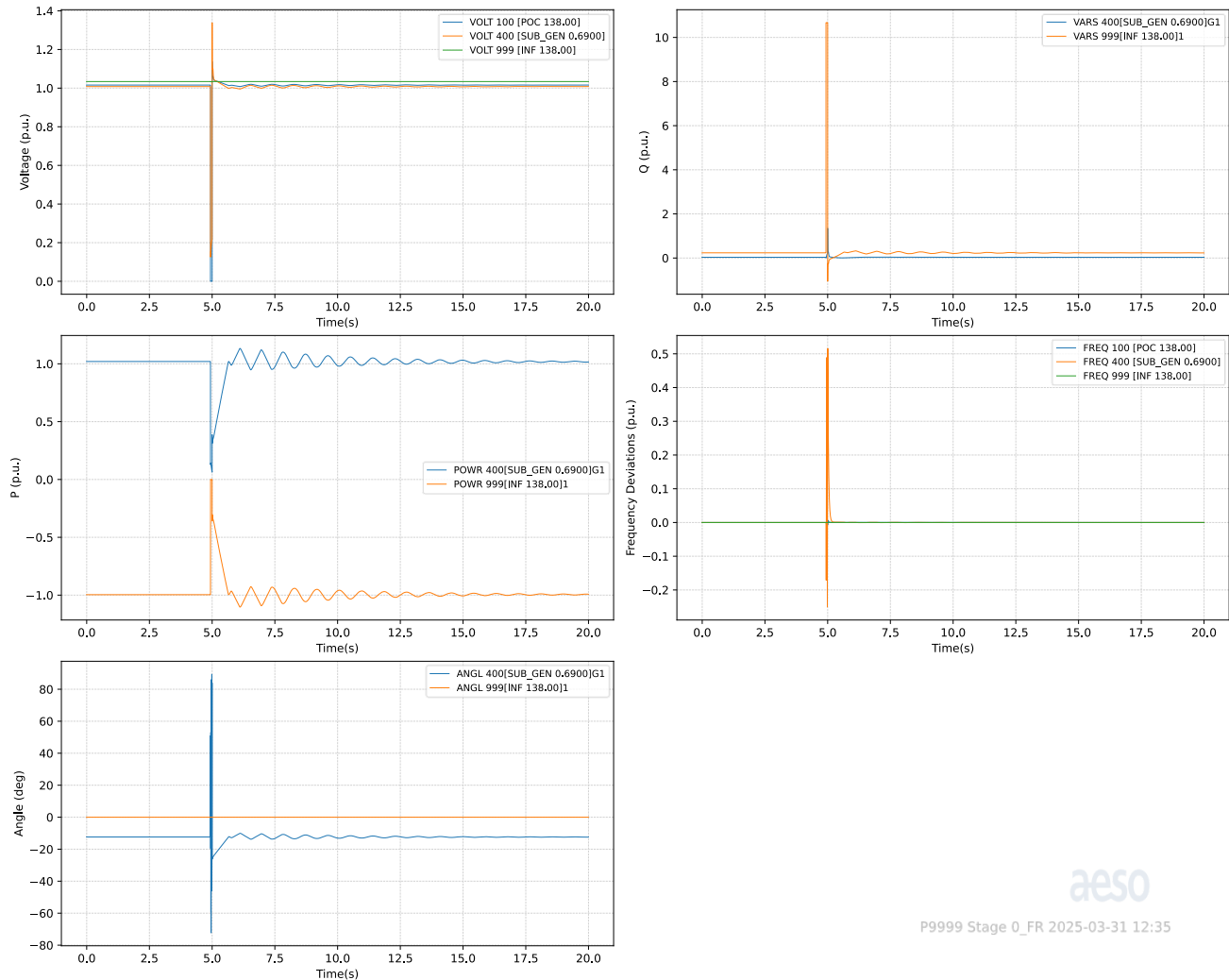


aeso
P9999 Stage 0_LFRT-IBR 2025-03-31 12:30

Figure 21 Sample LFRT test result

7.10 Fault recovery

In this test, a 6-cycle bus fault was applied at the Point of Connection (POC). Following fault clearance, both active and reactive power remained stable, with oscillations exhibiting effective damping.



aeso
P9999 Stage 0_FR 2025-03-31 12:35

Figure 22 Sample fault recovery test result

7.11 SCR

By conducting simulations across various Short Circuit Ratio (SCR) values, in this case [5, 3, 2, 1.5, 1], the generator remained online down and demonstrated stable operation to an SCR of 1.5. This indicates that the generator can maintain synchronism and stable performance in grid conditions with an SCR as low as 1.5. Therefore, the minimum SCR for stable operation of this generator is determined to be 1.5.

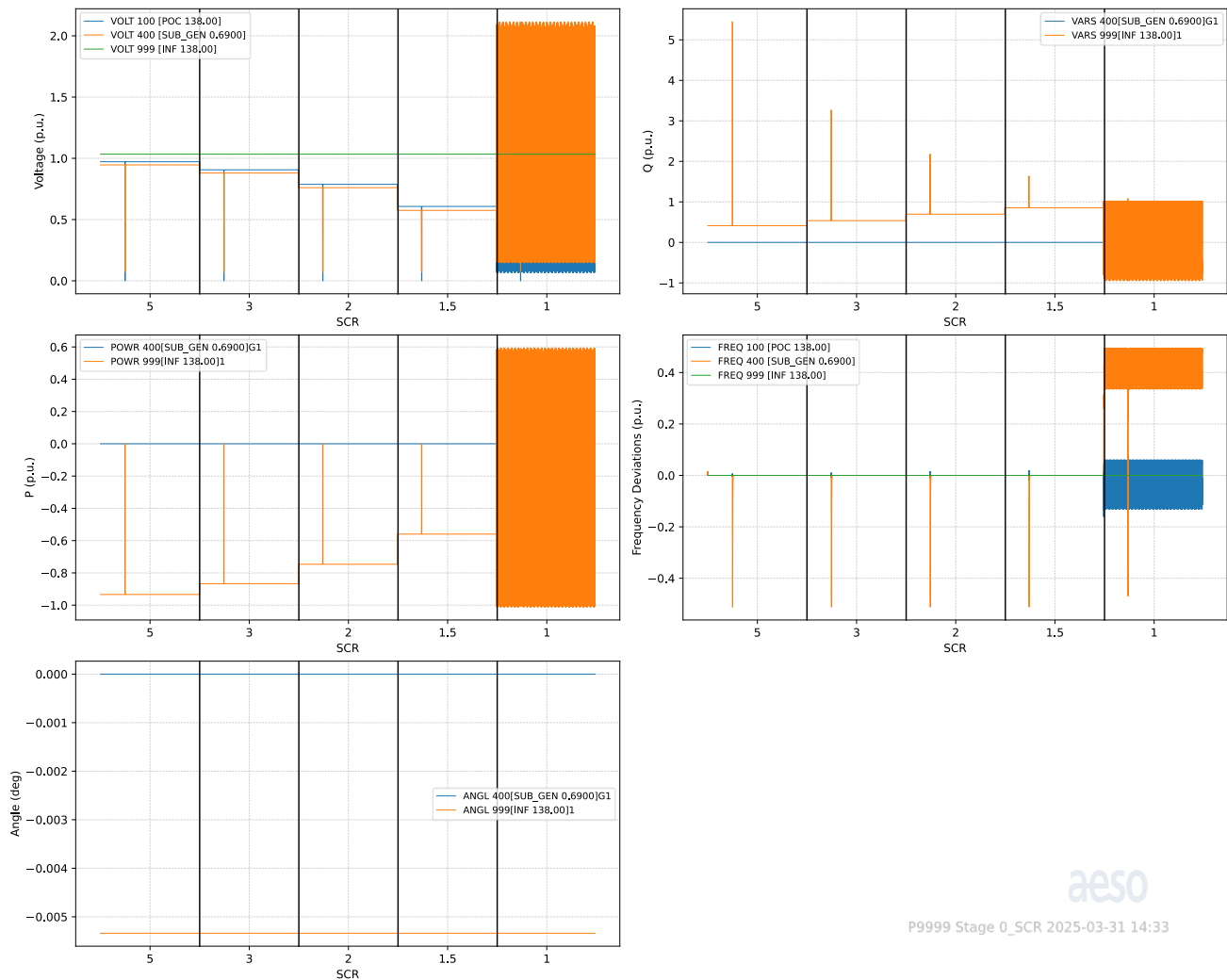
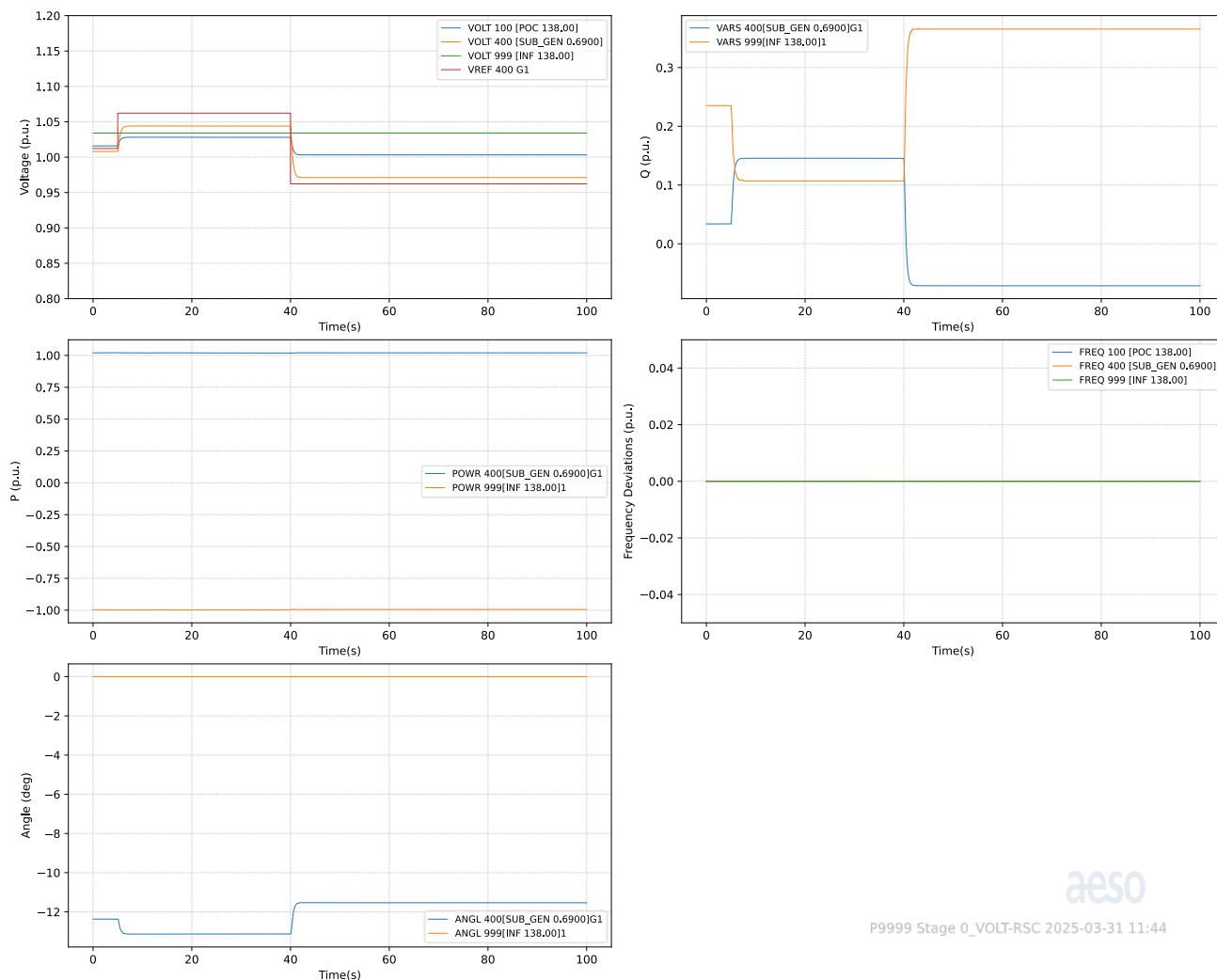


Figure 23 Sample SCR test results

7.12 Voltage reference step test

Under a +/-5% voltage reference step changes, the generator changes the reactive power output accordingly while real power is maintained.

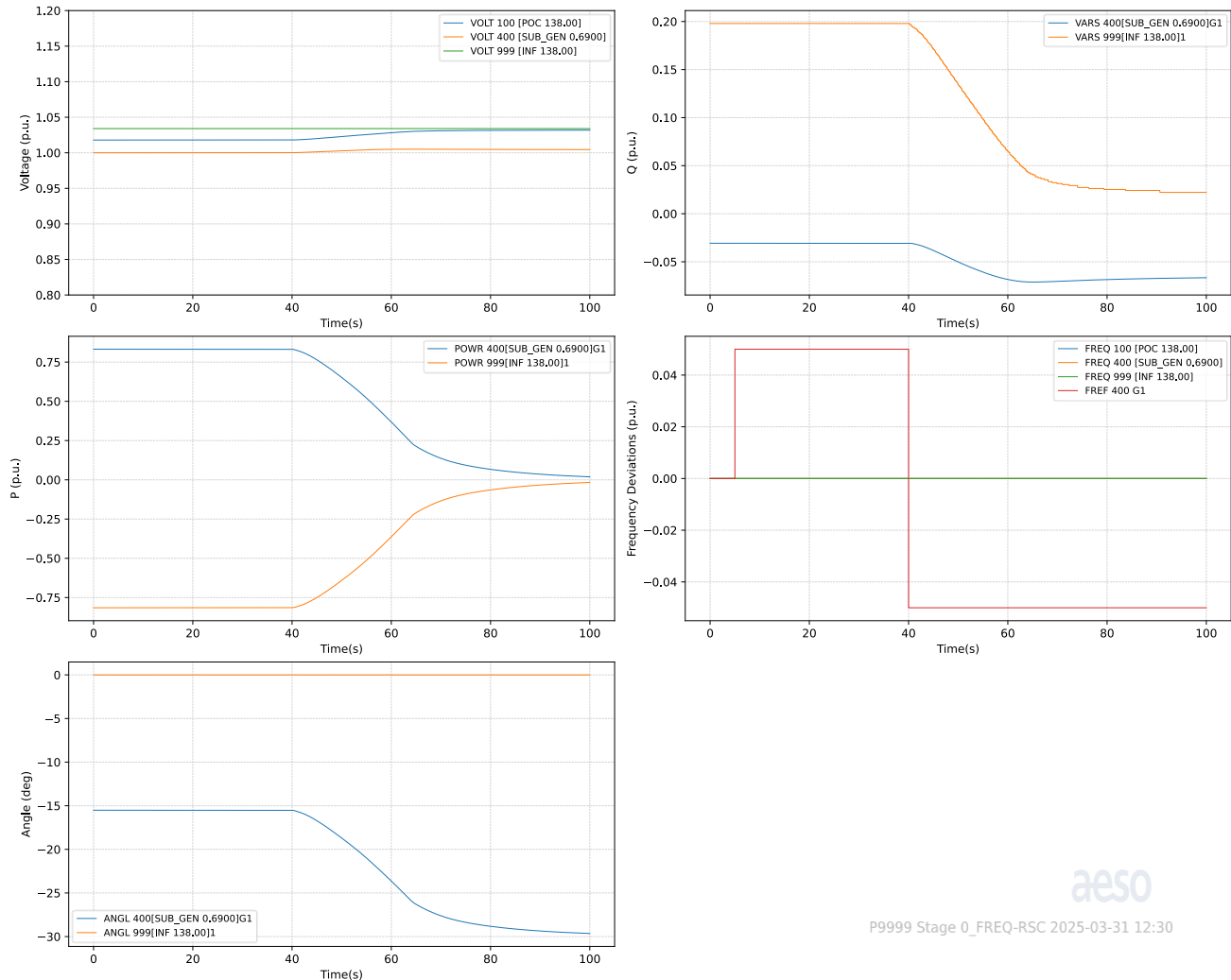


aeso
P9999 Stage 0_VOLT-RSC 2025-03-31 11:44

Figure 24 Sample voltage reference step test result

7.13 Frequency reference step test

In this test, real power is initialized at 80% of Pmax assumed in the power flow model. Under a +/-5% frequency reference step changes, the generator responds with active power changes accordingly. Since no headroom is reserved for underfrequency event, there is no change in active power during frequency reference step up.



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Figure 25 Sample frequency reference step test result