Alberta Electric System Operator
3000, 240 4 Avenue SW
Calgary, AB • T2P 4H4
aeso.ca

AESO PSSE Dynamic Model Performance Test Bench

Guideline

Date: April 9, 2025

Version: V1

Classification: Public

Contents

1. Background

The AESO PSS®E Dynamic Model Performance Test Bench is a tool developed by the Alberta Electric System Operator (AESO) to assist internal and external stakeholders in evaluating the performance of PSS®E dynamic models under various conditions and identifying potential modeling issues. This document provides guidance on case preparation and the effective use of the Test Bench.

2. Applicability

This Test Bench applies to all generation facilities and industrial complexes with generators at both transmission and distribution levels, including synchronous generators and inverter-based generators such as wind, solar and battery storage.

The test requirements are contained in the PDUP Checklist. Related references should be reviewed if applicable to the facility under study, which could include:

- AESO Connection Requirements for Inverter-Based Resources (February 2024)
- ID# 2010-001R Facility Modelling Data and List of Electrical and Physical Parameters for Transmission System Model
- ID# 2017-013R Model Validation and Reactive Power Reporting Guidance
- Section 503.4 Voltage Regulation
- Section 503.5 Voltage Ride Through
- Section 503.6 Frequency and Speed Governing
- AESO DER Roadmap Integration Paper - DER Ride-Through Performance Recommendations

3. Acronym

BESS - Battery energy storage system

DER - Distributed energy resource

IBRs - Inverter-based resources

OPBC - Operational Planning Base case

PBCS - Planning Base Case Suite

POC - Point of connection

SMIB - single machine infinite bus system

4. Running the Test Bench

4.1 Test Bench Prerequisites

The Model Performance Test Bench is an executable file (.exe) designed for use with PSS®E software. It is compatible with PSS®E versions 33, 34, and 35.

The release includes:

- Model Performance Test Bench (for PSS®E versions 33, 34)
- Model Performance Test Bench (for PSS®E version 35)
- InputSheet (.xlsx)
- PSS®E Dynamic Model Performance Test Bench Guideline

4.2 Preparing the Power flow base case

This Test Bench facilitates the evaluation of dynamic model performance using the isolated Single Machine Infinite Bus (SMIB) system.

The power flow cases shall be prepared as follow:

The test generation shall be modeled in the power flow case as follows: A slack bus with an infinite machine (large Mbase = 9999 MVA and small X_{source} = 0.01 pu) is connected to the generation facility via a zero-impedance tie line (X = 0.0001pu). The SMIB connections for different connection types and generation technologies are detailed below.

- For Inverter-based resources (IBRs) to comply with the "AESO Connection Requirements for Inverter-Based Resources", the SMIB system shall be connected to the Interconnection line of the generation facility, which connects to either a T-tap or a substation, depending on the configuration. The impedance of the interconnection line should be included based on the project's design specifications. If these specifications are unavailable, reasonable assumptions should be made to ensure accurate modeling.

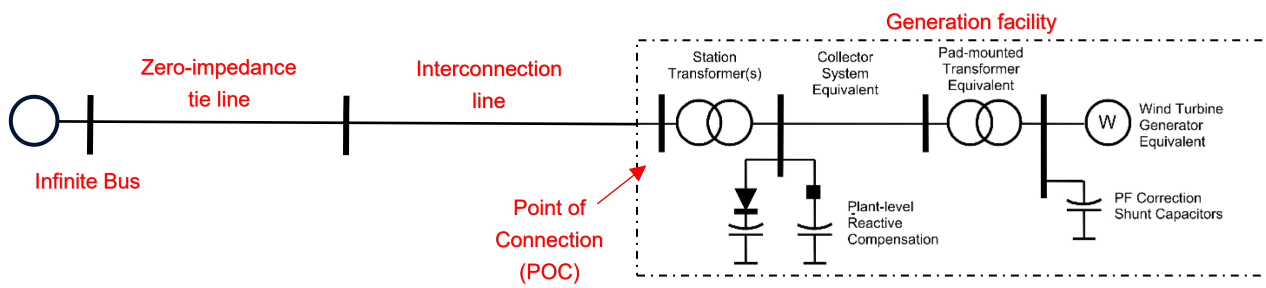

Figure 1 Network Diagram for IBRs comply with IBR connection requirement

- For Conventional machines or IBRs which are not required to comply with the "AESO Connection Requirements for Inverter-Based Resources", the SMIB system shall be connected to the POC of the generation facility.

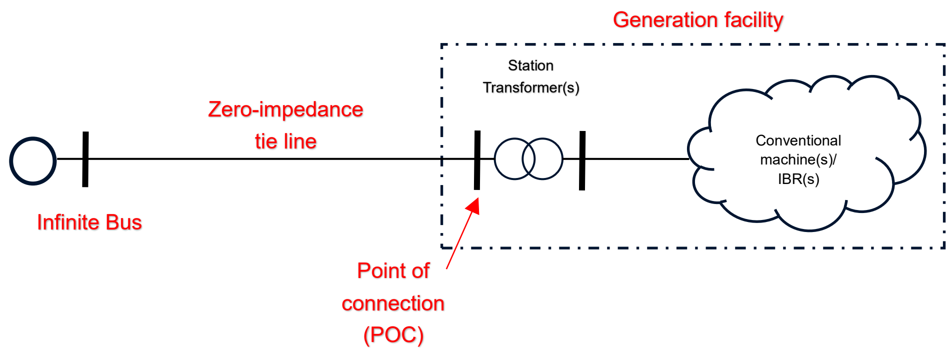

Figure 2 Network Diagram for conventional machine or IBRs not comply with IBR connection requirement

- For Distributed Energy Resources (DER) of any technology, the SMIB system shall be connected to the high voltage side of the grid-connected substation transformer. Detailed information for the substation transformer can be obtained from the Planning Base Case Suite (PBCS) or Operational Planning Base case (OPBC) which can be provided by the AESO on request.

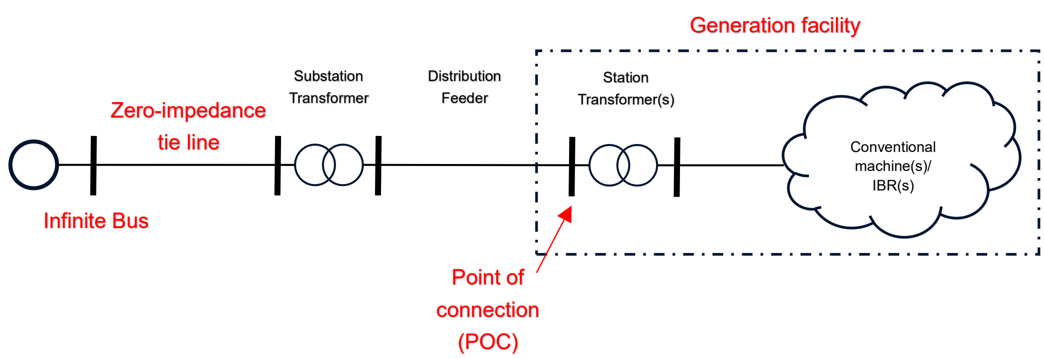

Figure 3 Network Diagram for DER

The DYR file of the test generation facility should align with the power flow case, with the following notes:

- Generator bus number and ID must match those in the power flow case.
- Model selection must correspond to the generator type/ technology based on the latest WECC approved model list (may be found on the WECC website), unless otherwise approved by AESO.
- A dynamic model of the infinite machine is not required.
- User-defined models are not supported.

4.3 Running the Test Bench

In the **InputSheet.xlsx** file, users can define input files, configure basic simulation settings, specify test cases, and select export formats directly within an.xlsx file. Each field is accompanied by detailed instructions to ensure easy and efficient completion.

4.3.1 Input files

In the *Input* section, users can define project details and specify input file locations. The Test Bench is designed to accept the following PSS®E file types, representing either the complete model with SMIB system or up to the Point of Connection (POC), as listed in Figure 4:

- Power Flow Data Files (.raw)
- Saved Case Files (.sav)
- Response Files (.idv)

INPUT FILES	This section enables the specification of the required file locations	
Project No.	Enter the 4 digit project ####	1234
Stage No.	Enter the 1 digit stage #	0
File Path	The complete path to the directory containing your input files	C:\MyProject
Output Folder	The name of the output folder for storing simulation results, located within the specified *File Path*	DYR_results
Facility Model	Accept any of the following file types: .idv, .raw, .sav of the complete test model or up to the Point of Connection (POC).	project.sav
Insert SMIB?	The program will insert SMIB to the most upstream bus of your facility	0
DYR Model	Accept : .dyr	project.dyr

Figure 4 Input file section

4.3.2 Simulation setup

In the *Simulation Setup* section, the user shall specify the simulation parameters as shown in Figure 5. This includes:

- **Simulation time step (DELT):** Set to $\frac{1}{4}$ cycle by default.
- **System transformer high-voltage side voltage range:** By default, configured between 69 kV and 500 kV to assist the tool in identifying the point of connection for the generating facility.
- **Generation Active Power Output:** Specified in per unit (pu), ranging between 0 and 1.
- **Battery Energy Storage System (BESS) Active Power Output:** Defined in per unit (pu), with negative values indicating charging mode and positive values indicating discharging mode.
- **Motor Active Power Consumption:** defined in per unit (pu) with negative values.
- **Infinite Bus Voltage:** Represents the system's normal operating voltage in per unit
- **Interconnection Line Impedance:** In the simulation setup for inverter-based resources (IBRs), there is an option to include the interconnection line when creating the base case. By setting this field to any value greater than 0, the interconnection line is incorporated into the model if the generating facility is represented up to the Point of Connection (POC). For conventional machines or DERs, set this value to 0. Do not leave it empty as it will trigger an error.

BASIC SIMULATION SETUP		
Simulation Time Step	Simulation time step in seconds	0.0041667
Simulation Duration	Minimum simulation duration in seconds	20
System transformer voltage lower bound	This is used to identify the Point of Connection (POC), defined as the high-voltage side of the system transformer for the facility under test. Specify the lower bound in kV.	69
System transformer voltage upper bound	This is used to identify the Point of Connection (POC), defined as the high-voltage side of the system transformer for the facility under test. Specify the higher bound in kV.	500
Enable Setup	Set to 1 to enable the following settings or 0 to disable them if a test case is already available. If this is disabled, Insert SMIB will be automatically disabled.	1
GEN P%	Initial Pgen as a percentage of Pmax (+) A machine with Pmin >= 0 is treated as a regular GEN	1
BESS P%	Initial Pgen as a percentage of the Pmax (+), Pmin (-) A machine with Pmin < 0 and Pmax > 0 is treated as a BESS	1
MOTOR P%	Initial Pgen as a percentage of Pmin (-) A machine with Pmin < 0 and Pmax = 0 is treated as a Motor	1
Inf Bus Voltage	Initial voltage of the infinite bus. This may be set to the nominal voltage specific to the service area (i.e. For service areas with a voltage level of 144 kV, set it to 144 / 138 = 1.043	1
Interconnection Line Impedance	The impedance of the line between the **high side of the system transformer and the tap point** is defined here. A value of **0** indicates that no line is required for the tests, typically applicable to conventional machines or DERs. For IBRs, if the exact impedance is unavailable, a default value of **0.01** may be used.	0

Figure 5 Simulation setup section

4.3.3 Specify AESO dynamic model performance tests

The *Tests* section outlines the model performance evaluations detailed in Table 1 and Figure 6.

For voltage (VOLT) and frequency (FREQ) tests, the PLBVFU1 model is used at the infinite machine to play back voltage and frequency signals defined in the respective sheets of the InputSheet.xlsx file. Each sheet is named after the corresponding test listed in the *Test* section. For voltage and frequency ride-through test, please refer to the PDUP Checklist for requirements specific to the generation type.

For Fault recovery test (FR) and Reference setpoint step test (RSC), refer to section 5.2 to determine the system Thevenin equivalent reactance for the zero-impedance tie line.

Notation	Test Type
FS	Flat start
VOLT	Voltage response tests (Voltage step up and down, voltage ride through)
FREQ	Frequency response tests (Frequency step up and down, frequency ride through)
FR	Fault recovery test
SCR	Short-circuit ratio test – Intended for transmission connected IBRs
RSC	Reference setpoint step test (Voltage reference, Frequency reference) – Intended for transmission connected IBRs.

Table 1 Performance test type

TESTS	Enter '1' for each test below that needs to be run. The voltage and frequency profile tab is assigned and can be modified as needed. - For the **Fault Recovery (FR) Test**, enter the *system equivalent reactance* for the zero impedance tie line in per unit (pu) and the fault duration in seconds within square brackets. The *system equivalent reactance* should be determined using the latest OPBC case. If this information is unavailable, it may be approximated using SCR = 3 for IBRs or SCR = 5 for conventional generators, using the following formula: X_pu = 1/ (SCR X P_pu) where P_pu is the maximum active power output of the tested power plant at the Point of Connection (POC), based on a 100MVA base. - For the **Short Circuit Ratio (SCR) Test**, enter the SCR values within square brackets. Note this test only applies to IBRs. - For the **Reference Step Change (RSC) Test**, enter the reference type (VOLT-RSC, or FREQ-RSC) in quotations, the system equivalent impedance for the zero impedance tie line in per unit (pu), and the step change percentage within square brackets. The *system equivalent reactance* can be estimated using the same method as the FR Test. Note these tests only apply to IBRs. Add more tests by inserting rows within this section.	
FS	FS	1
FREQ	FRQ-STEP-UP	1
FREQ	FRQ-STEP-DOWN	1
VOLT	VLT-STEP-UP	1
VOLT	VLT-STEP-DOWN	1
VOLT	HVRT-IBR	1
VOLT	LVRT-IBR	1
FREQ	HFRT-IBR	1
FREQ	LFRT-IBR	1
FR	[0.1, 0.066667]	1
SCR	[8,5,3,2,1.9,1.7,1.5,1.3]	1
RSC	['VOLT-RSC', 0.01, 0.05]	1
RSC	['FREQ-RSC', 0.01, 0.05]	1

Figure 6 Performance test section

4.3.4 Specify output file format

Simulation outputs are saved in .sav and .pdf formats. Additionally, the *Export* section allows for the inclusion of .csv and .svg output formats, as shown in Figure 7.

EXPORT	The following files will be automatically saved: the test case in .raw or .sav, result plots in a .pdf file, and simulation data in .out format. Additionally, you have the option to save the data in .csv format.	
.csv	dynamic simulation results	1
image	dynamic simulation result plots	1

Figure 7 Export section

4.3.5 Run tests

To execute the Dynamic model performance tests:

1. Enable the Run: Set “Run Status” to 1 to enable the simulation run, as illustrated in Figure 8. If set to 0, model performance tests will not run. If multiple scenarios are being utilized for the

project and the same tests need to be run, assign a unique name to each output folder to differentiate simulation results.

2. Launch the Executable**:** Open the AESO_MPTB.exe file for your specific PSS®E version.
3. Select PSS®E Version: Within the application, choose the appropriate PSS®E version from the available options.
4. Load Input File: Click on "Browse Input File" and navigate to select the InputSheet.xlsx file containing your test configurations.

INPUTS	NOTES			
Run Status	Set to 0 to disable a round while preserving setting records	1	0	0
INPUT FILES	This section enables the specification of the required file locations			
Project No.	Enter the 4 digit project ####	1234	1234	1234
Stage No.	Enter the 1 digit stage #	0	0	0

Figure 8 Run Status to enable simulation run

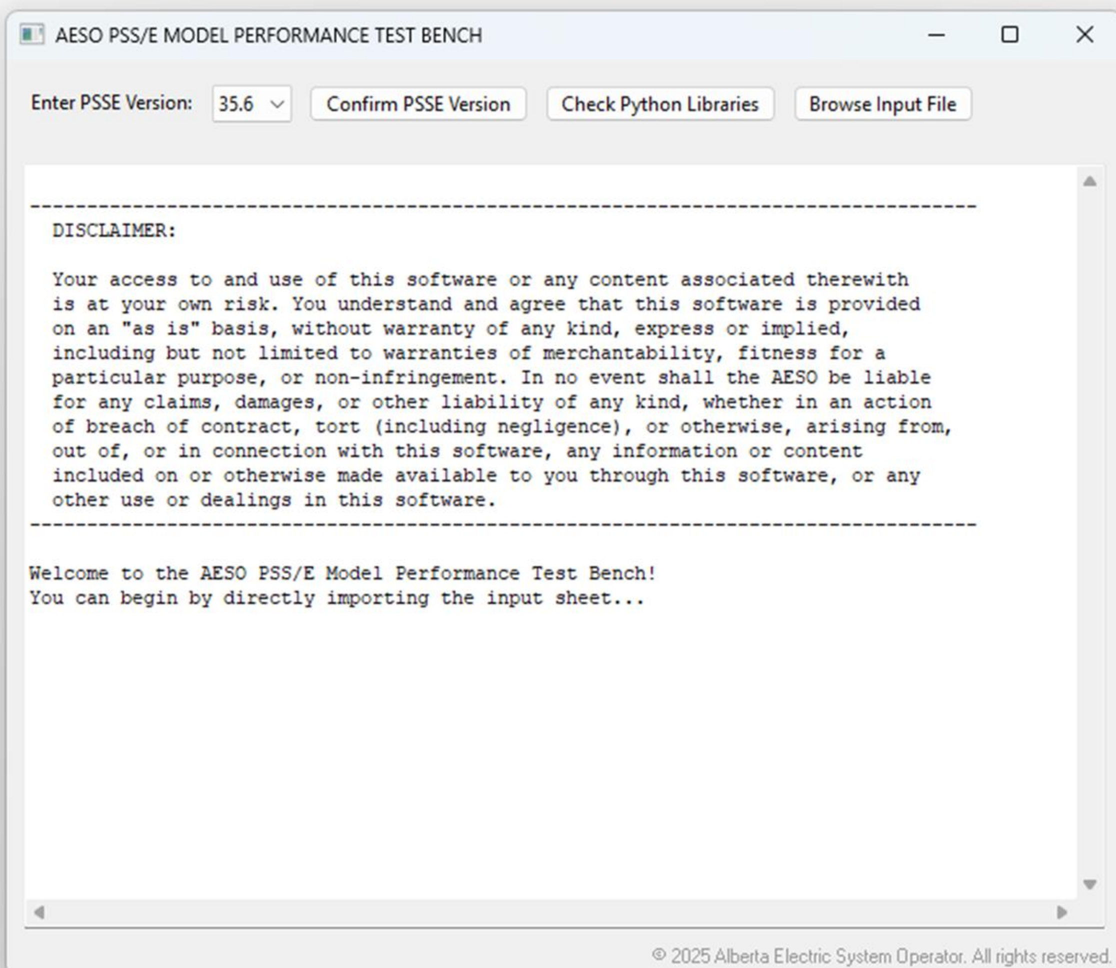

Figure 9 Model Performance Test Bench

4.4 Output files

The *Results* folder is created within the directory specified in the *Input* section, as illustrated in Figure 10. Figure 10This folder contains subdirectories named according to each test type, which include the following output files:

- test case (.raw)
- converted case (.sav)
- snap file (.snp)
- PSS/E log file
- outfile (.out)
- result pdf (.pdf)
- output file (.csv) – optional
- result image (.svg)

Additionally, the program's run-time log files can be found in the *AESO_MPTB_RUN_LOG* folder, located in the same directory as the *.exe* file.

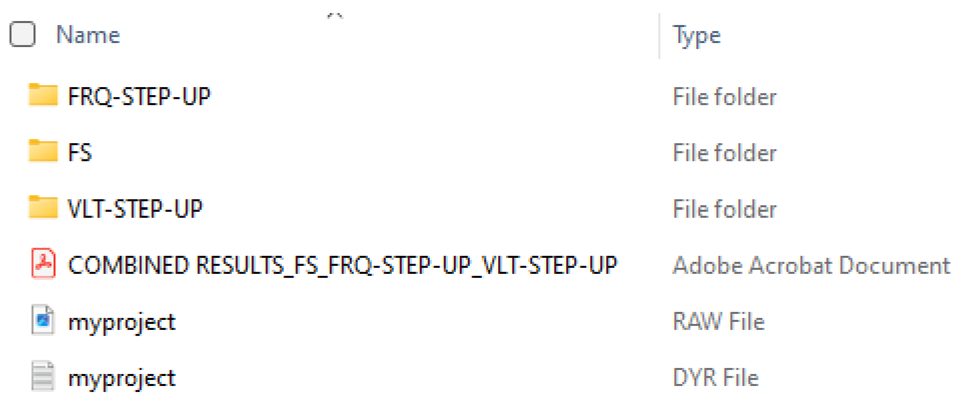

Figure 10 Result folder structure

The following signals will be monitored in the simulations and saved in the output file. These monitored signals are essential for analyzing the dynamic performance and stability of the power system during various operating conditions and disturbances.

- **Active power:** The real power output of the test generators and infinite machine, measured in per unit.
- **Reactive power:** The reactive power output of the test generators and infinite machine, measured in per unit.
- **Bus angle:** The angle magnitude at generator bus, POC and infinite bus, measured in degree
- **Bus voltage:** The voltage magnitude at generator bus, POC and infinite bus, measured in per unit
- **Bus frequency**: The frequency magnitude at generator bus, POC and infinite bus, measured in per unit

The result PDF shall be stamped and sealed by a professional engineer with APEGA and shall be included in the submission of the PUDP and the PUDP Checklist.

5. Additional Information

5.1 Short circuit ratio test

This test will demonstrate transmission connected IBR facility performance under weak grid conditions given system strength at POC is subject to variation triggered by outages, network reconfiguration, etc. The model shall be tested for a set of short circuit ratios (SCRs) at the POC starting from a strong system condition and moving towards a weaker condition. The SCR adjustment is achieved by varying the reactance of the zero-impedance tie line. The simulation starts at a pre-defined SCR followed by applying a solid three phase to ground fault at the POC which will be cleared after 6 cycles. The SCR will then be changed to a lower value and the fault will be applied again at a time interval of 5 seconds, and so on. The default settings of the SCR input are [8,5,3,2,1.9,1.7,1.5,1.3]. SCR[1] is calculated as follows:

$$SCR = \frac{SCMVA}{MW^{IBR}}$$

$SCMVA$ = The short circuit MVA level at the POC without the current contribution of the IBR.

MW^{IBR} = Nominal power rating of the IBR facility at the POC. The test bench assumes that losses and station service loads within the generating facility are negligible, and the total P_{max} of the facility's generators, as specified in the power flow model, is used for the calculation.

Consider an example of a facility comprising wind generation (P_{max} = 80 MW) and a BESS with a maximum discharge power of 20 MW and a minimum charge power of -19 MW, operating with an SCR of 5. The reactance of the zero-impedance tie line - representing the system's equivalent reactance - is calculated below based on the nominal power rating of the IBR facility at the POC and shall be used for testing scenarios where the BESS operates in either charging or discharging mode.

$$SCMVA = SCR \times \sum P_{gi} = 5 \times (80 + 20) = 500$$

$$System\ equivalent\ reactance = \frac{system\ MVA}{SCMVA} = \frac{100}{500} = 0.2\ pu$$

5.2 System Thevenin equivalent impedance

The zero-impedance tie line reactance shall be modified to the System Thevenin equivalent reactance for fault recovery tests and reference setpoint step tests. The System Thevenin equivalent reactance can be determined in the latest PBCS or OPBC with the generation facility modelled. If this detail is unavailable, appropriate assumptions should be made to ensure accurate modeling.

[1] AESO, "AESO 2023 Reliability Requirements Roadmap", March 10, 2023

6. Troubleshooting

This section offers a comprehensive overview of common errors encountered while using the tool, along with their respective resolutions. Its primary objective is to assist users in efficiently diagnosing and addressing these issues.

1. Error messages can be found in the run-time log files located in the *AESO_MPTB_RUN_LOG* folder, which can assist with troubleshooting the simulations.
2. When encountering pop-up messages in PSS®E indicating a floating-point (divide-by-zero/ overflow) failure as illustrated in Figure 11, it often signifies errors within the dynamic model. To address this issue, please thoroughly review the dynamic model to ensure its accuracy and correctness. Such failures can occur due to improper data inputs, incompatible model parameters, or issues related to the software's handling of floating-point arithmetic.

```
-------------FS-------------
Floating-Point Divide-By-Zero.
Image              PC                Routine             Line     Source
dstbl.dll          00007FFE6C240B64  IEEG1Z               331     IEEEG1.F
dsmdl.dll          00007FFE6FFA763B  IEEEG1SDU             35     ieeeg1du.for
PTIUtils.dll       00007FFF05BF223C  Unknown          Unknown     Unknown
dstbl.dll          00007FFE6BF79489  Unknown          Unknown     Unknown
dstbl.dll          00007FFE6BF70E43  TBLCNC              1608     tabldy.for
psseng.dll         00007FFE5676396C  Unknown          Unknown     Unknown
psseng.dll         00007FFE5675FD29  Unknown          Unknown     Unknown
psspyc.pyd         0000020AA2BF630A  Unknown          Unknown     Unknown
python39.dll       00007FFED0568AB9  Unknown          Unknown     Unknown
python39.dll       00007FFED0515215  Unknown          Unknown     Unknown
python39.dll       00007FFED05F3C1F  Unknown          Unknown     Unknown
python39.dll       00007FFED06F86FF  Unknown          Unknown     Unknown
python39.dll       00007FFED06F96F6  Unknown          Unknown     Unknown
python39.dll       00007FFED0660CC7  Unknown          Unknown     Unknown
pydevd_frame_eval  00007FFF1E948BBE  Unknown          Unknown     Unknown
python39.dll       00007FFED051D06F  Unknown          Unknown     Unknown
python39.dll       00007FFED051C97B  Unknown          Unknown     Unknown
python39.dll       00007FFED05F3BE4  Unknown          Unknown     Unknown
python39.dll       00007FFED06F86FF  Unknown          Unknown     Unknown
python39.dll       00007FFED06F963E  Unknown          Unknown     Unknown
python39.dll       00007FFED0660CC7  Unknown          Unknown     Unknown
pydevd_frame_eval  00007FFF1E948BBE  Unknown          Unknown     Unknown
python39.dll       00007FFED051D06F  Unknown          Unknown     Unknown
python39.dll       00007FFED051C97B  Unknown          Unknown     Unknown
python39.dll       00007FFED05F3BE4  Unknown          Unknown     Unknown
python39.dll       00007FFED06F86FF  Unknown          Unknown     Unknown
python39.dll       00007FFED06F963E  Unknown          Unknown     Unknown
```

Figure 11 PSS®E floating point failure

3. Plotting errors might occur if the .out file is opened during the simulation as shown in Figure 12.

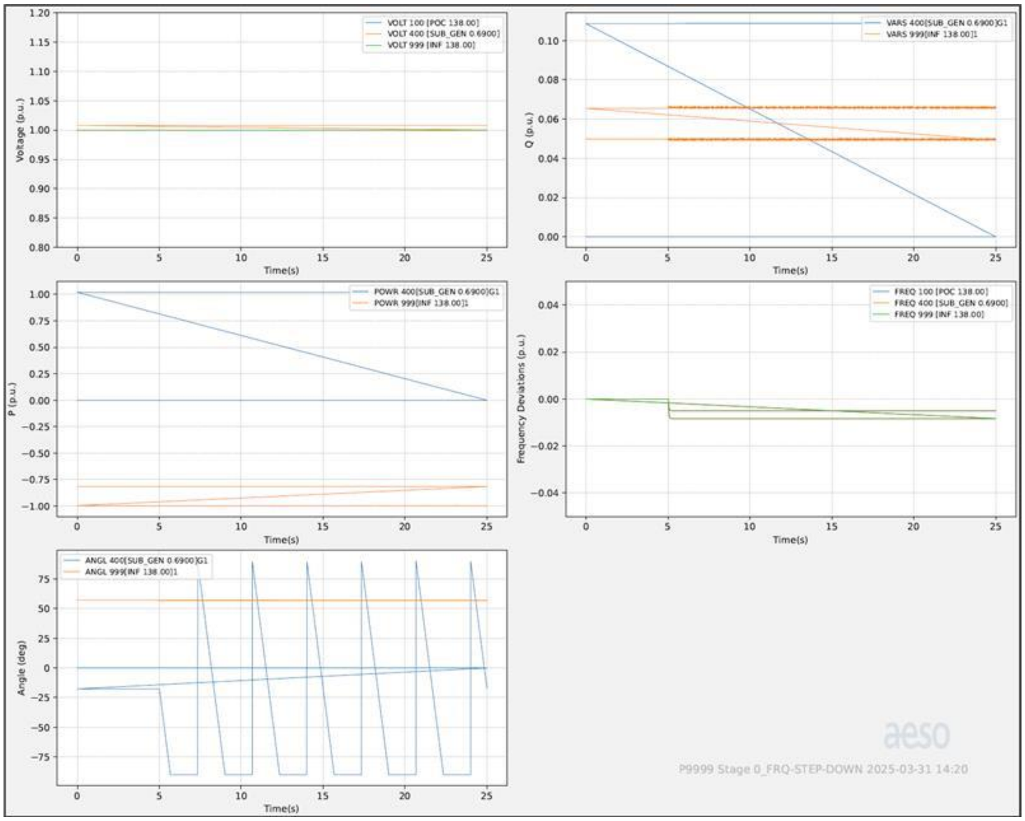

Figure 12 Sample plotting error results

7. Sample Results

Followings are the sample model performance test results of an IBR (wind) facility. For more detail on the test requirements and acceptance criteria correspond to the generation technology, connection type and project stages, please refer to the PDUP Checklist.

7.1 Flat Start

Flat start test showing steady generator voltage, real and reactive power flow.

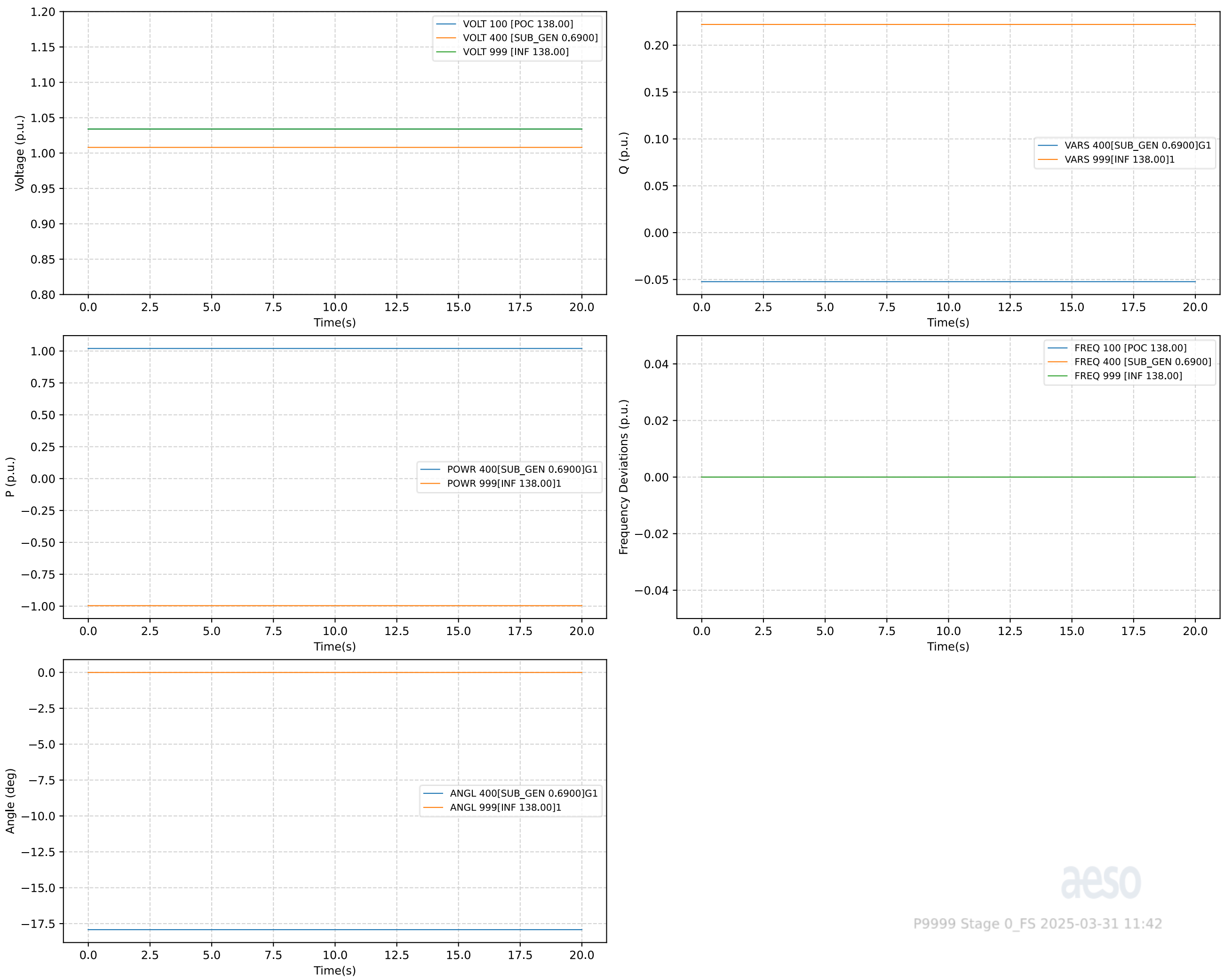

Figure 13 Sample flat start test result

7.2 Voltage step-down test

Under a 5% voltage step down at the POC, the generator increased reactive power output and maintained real power.

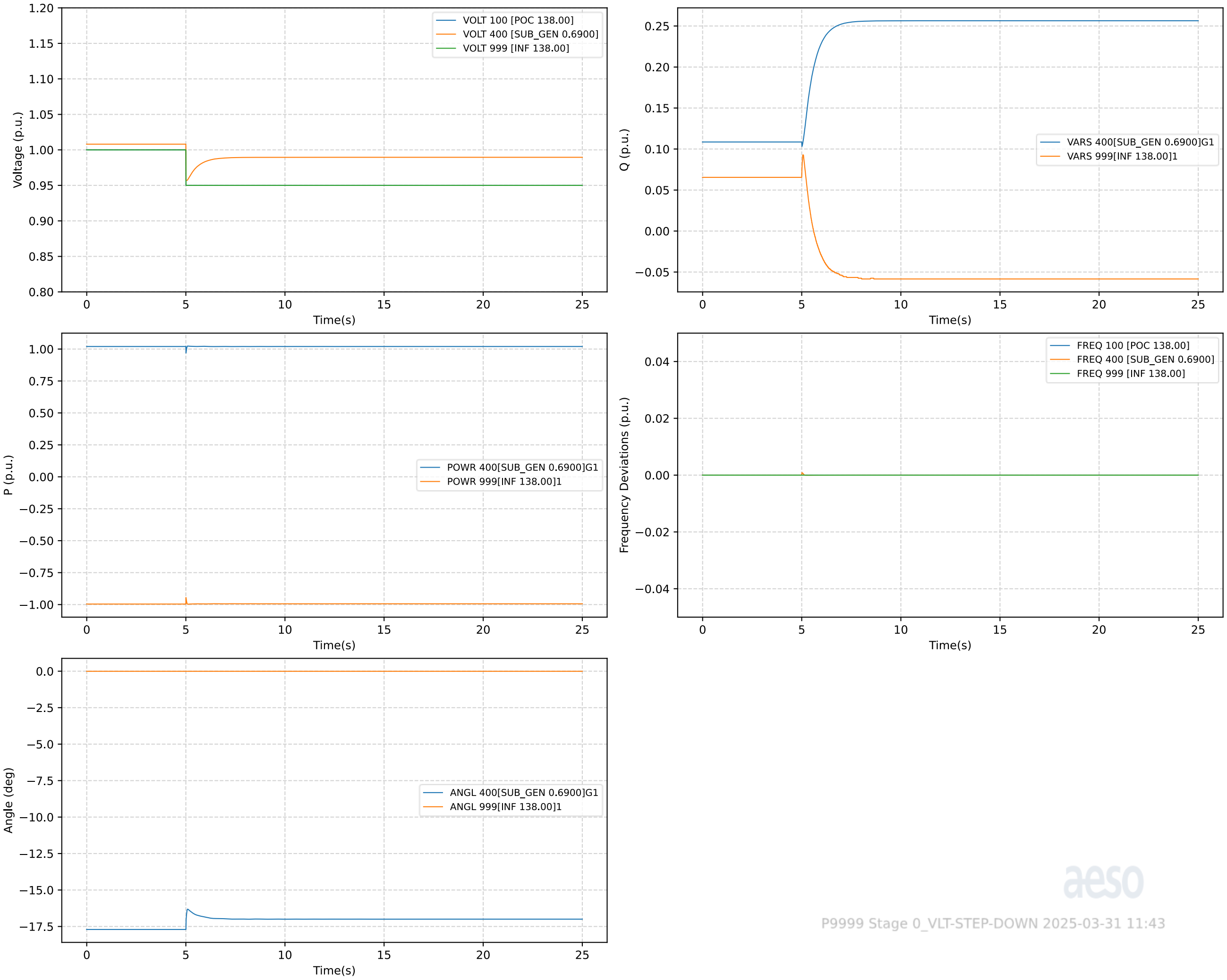

Figure 14 Sample voltage step down test result

7.3 Voltage step-up test

Under a 5% voltage step up at the POC, the generator decreased reactive power output and maintained real power.

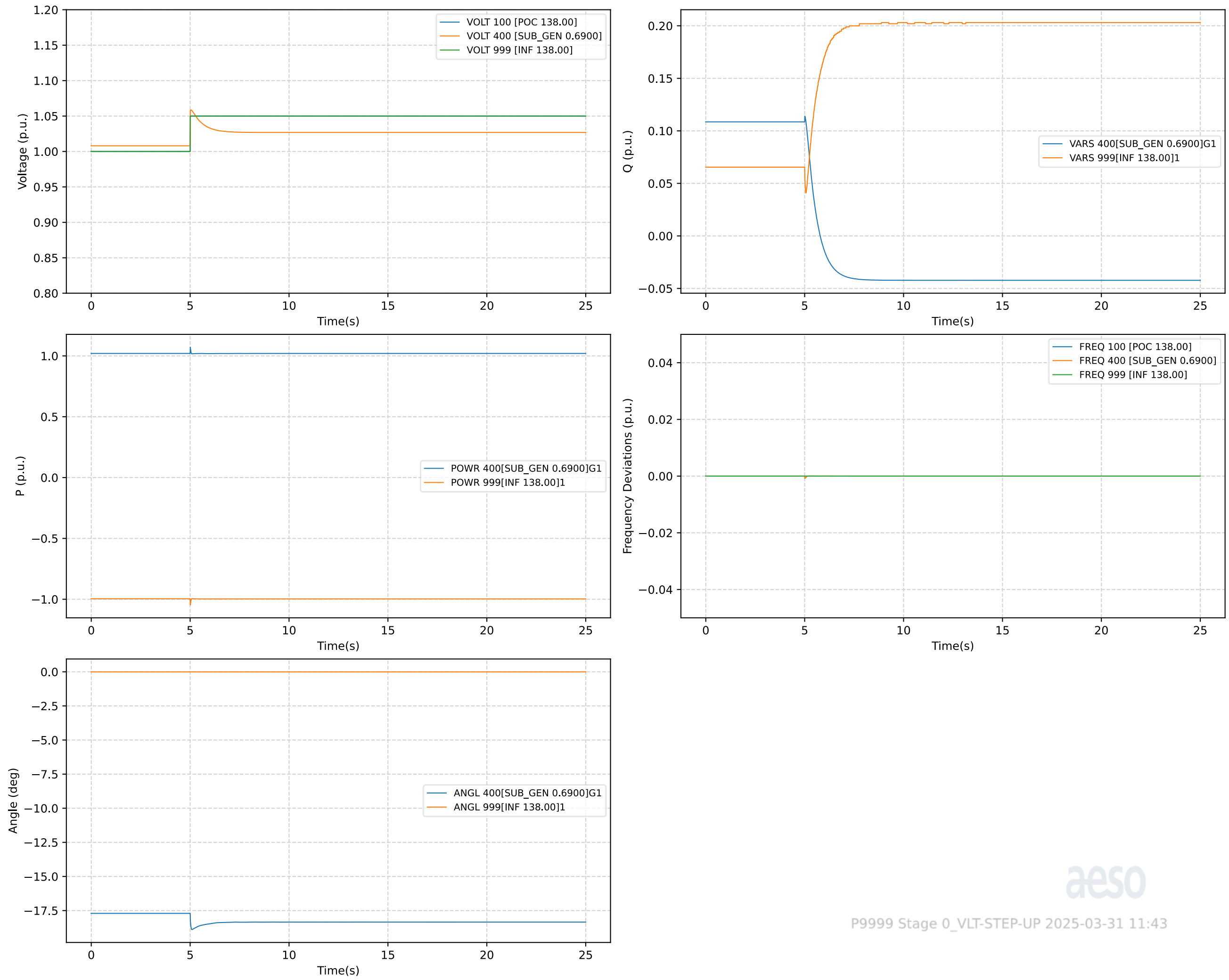

Figure 15 Sample voltage step up test result

7.4 Frequency step-down test

In this test, real power is initialized at 80% of Pmax assumed in the power flow model. For a 0.5% (0.3Hz) decrease in frequency, real power is maintained assuming there is no headroom to increase real power.

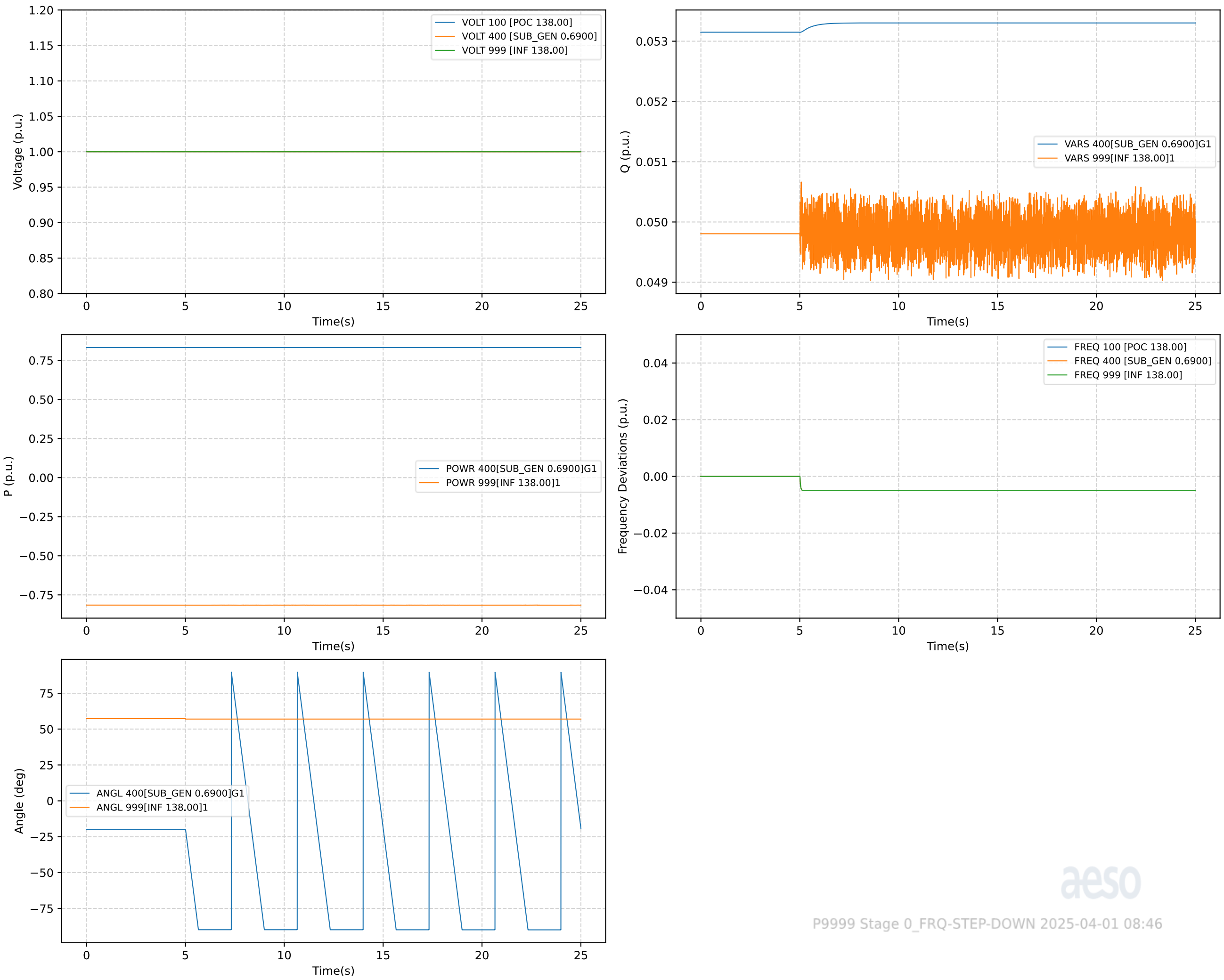

Figure 16 Sample frequency step-down test result

7.5 Frequency step-up test

In this test, real power is initialized at 80% of Pmax assumed in the power flow model. For a 0.5% (0.3Hz) increase in frequency, real power output of the generator decreased.

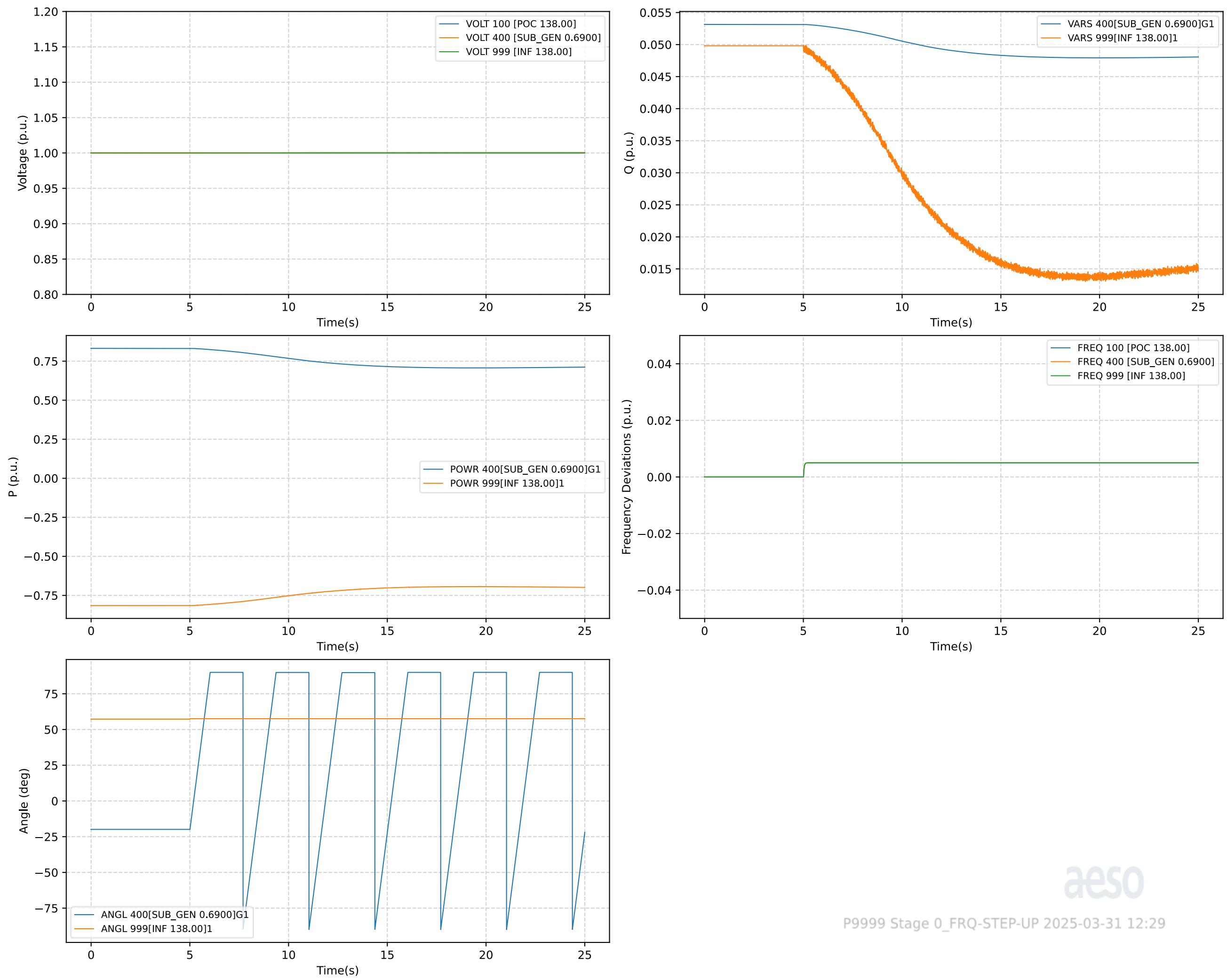

Figure 17 Sample frequency step-up test result

7.6 High voltage ride-through (HVRT) test

Under the variations of voltages under HVRT specified in the IBR connection requirement, the real power is maintained, and the reactive power absorption decreases in response to the high voltage transient.

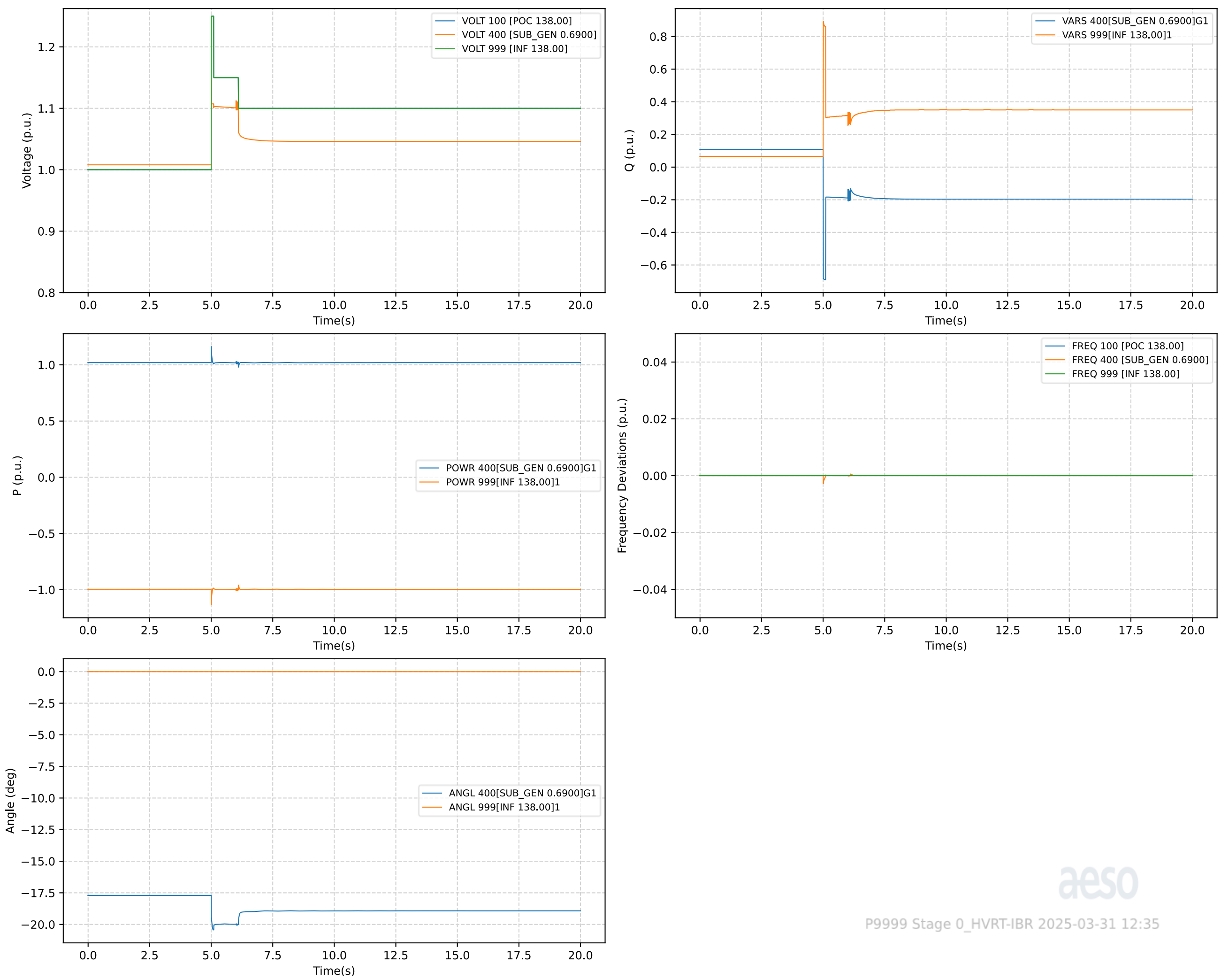

Figure 18 Sample HVRT test result

7.7 Low voltage ride-through (LVRT) test

Under the variations of voltages under LVRT specified in the IBR connection requirement, reactive power absorption increases in response to the high voltage transient. Active power recovery is acceptable.

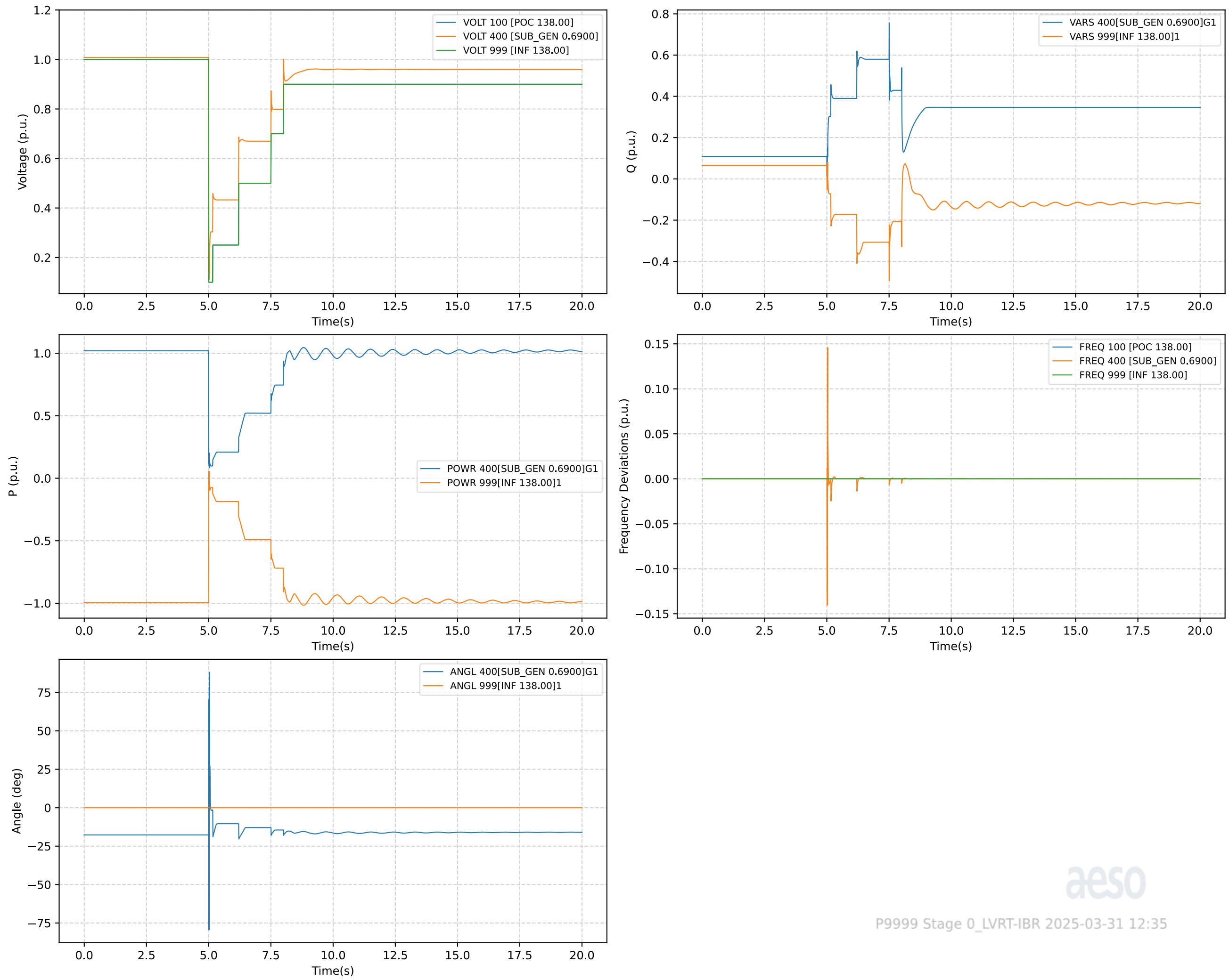

Figure 19 Sample LVRT test result

7.8 High frequency ride-through (HFRT) test

In this test, real power is initialized at 80% of Pmax assumed in the power flow model. Under the variations of voltages under HFRT specified in the IBR connection requirement, the real power output decreased according to the frequency variation.

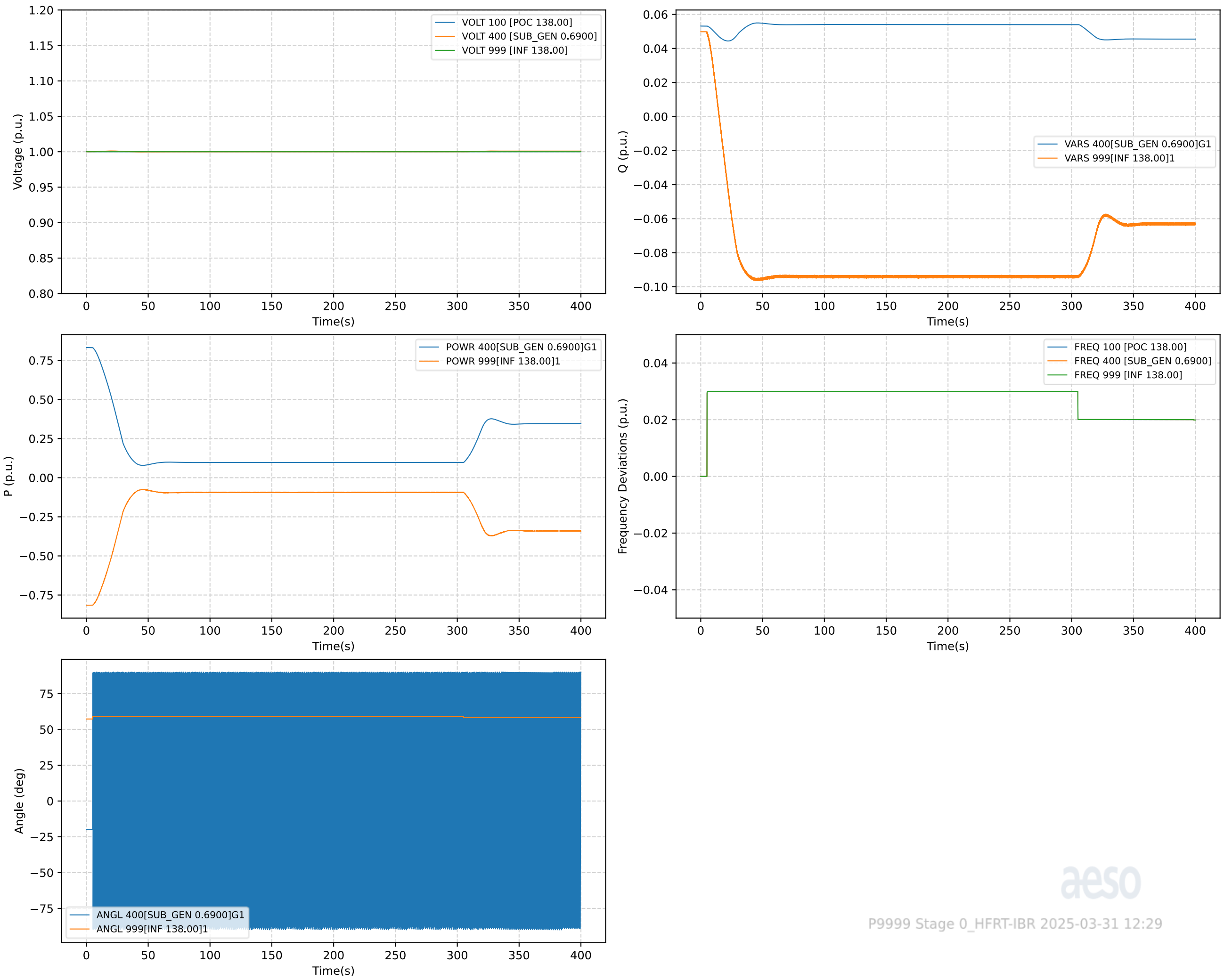

Figure 20 Sample HFRT test result

7.9 Low frequency ride-through (LFRT) test

In this test, real power is initialized at 80% of Pmax assumed in the power flow model. Under the variations of voltages under LFRT specified in the IBR connection requirement, the real power output remained constant assuming no headroom is reserved.

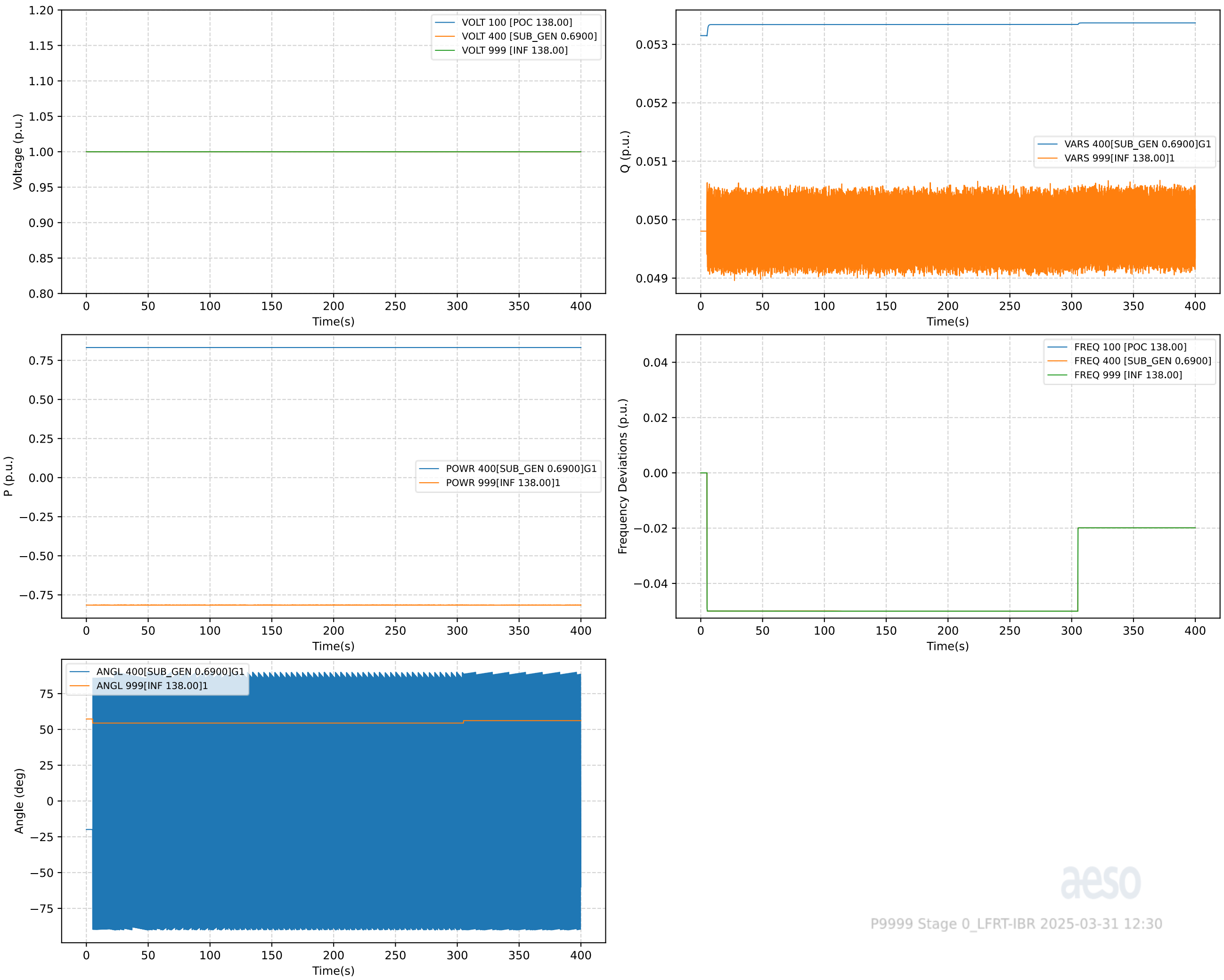

Figure 21 Sample LFRT test result

7.10 Fault recovery

In this test, a 6-cycle bus fault was applied at the Point of Connection (POC). Following fault clearance, both active and reactive power remained stable, with oscillations exhibiting effective damping.

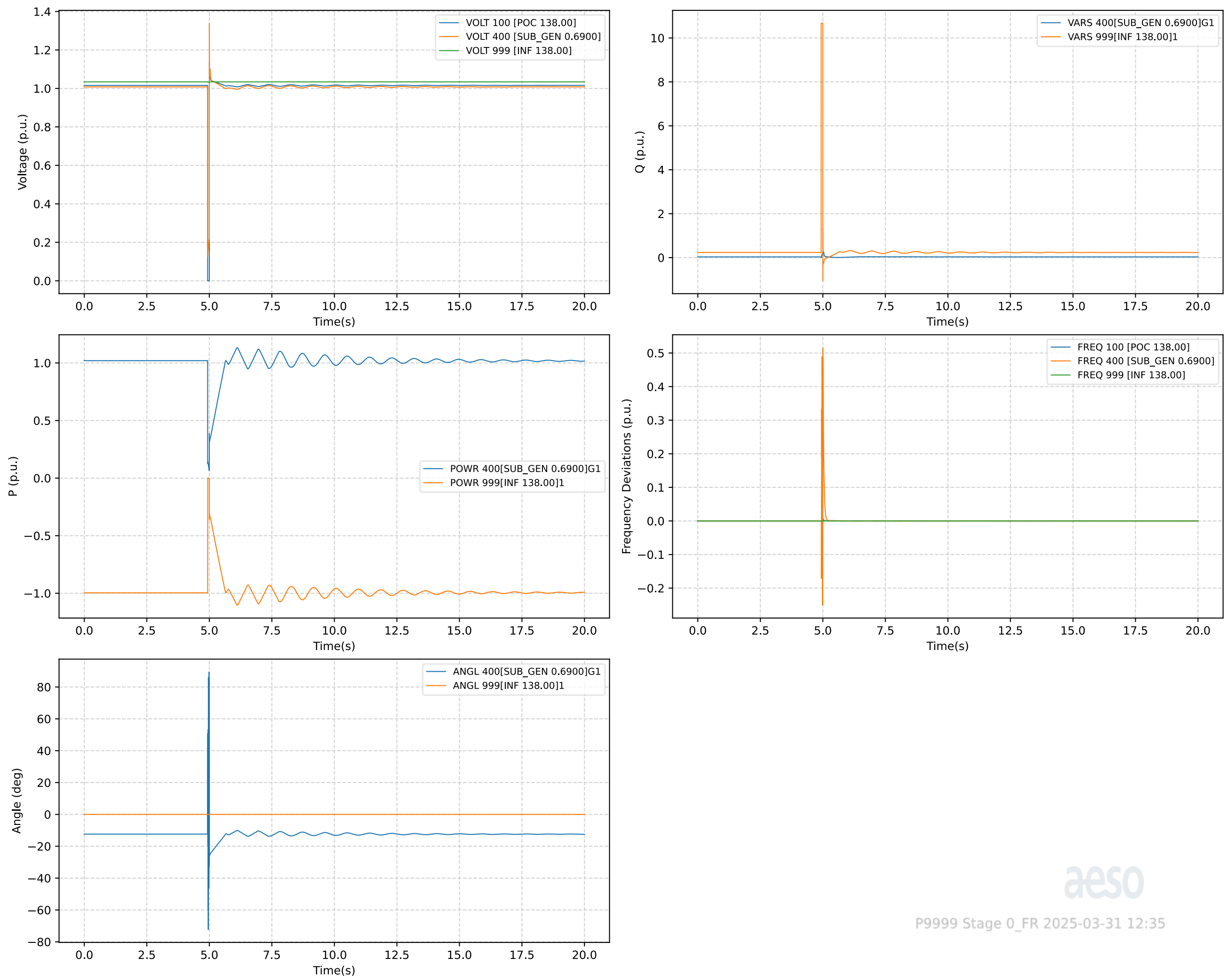

Figure 22 Sample fault recovery test result

7.11 SCR

By conducting simulations across various Short Circuit Ratio (SCR) values, in this case [5, 3, 2, 1.5, 1], the generator remained online down and demonstrated stable operation to an SCR of 1.5. This indicates that the generator can maintain synchronism and stable performance in grid conditions with an SCR as low as 1.5. Therefore, the minimum SCR for stable operation of this generator is determined to be 1.5.

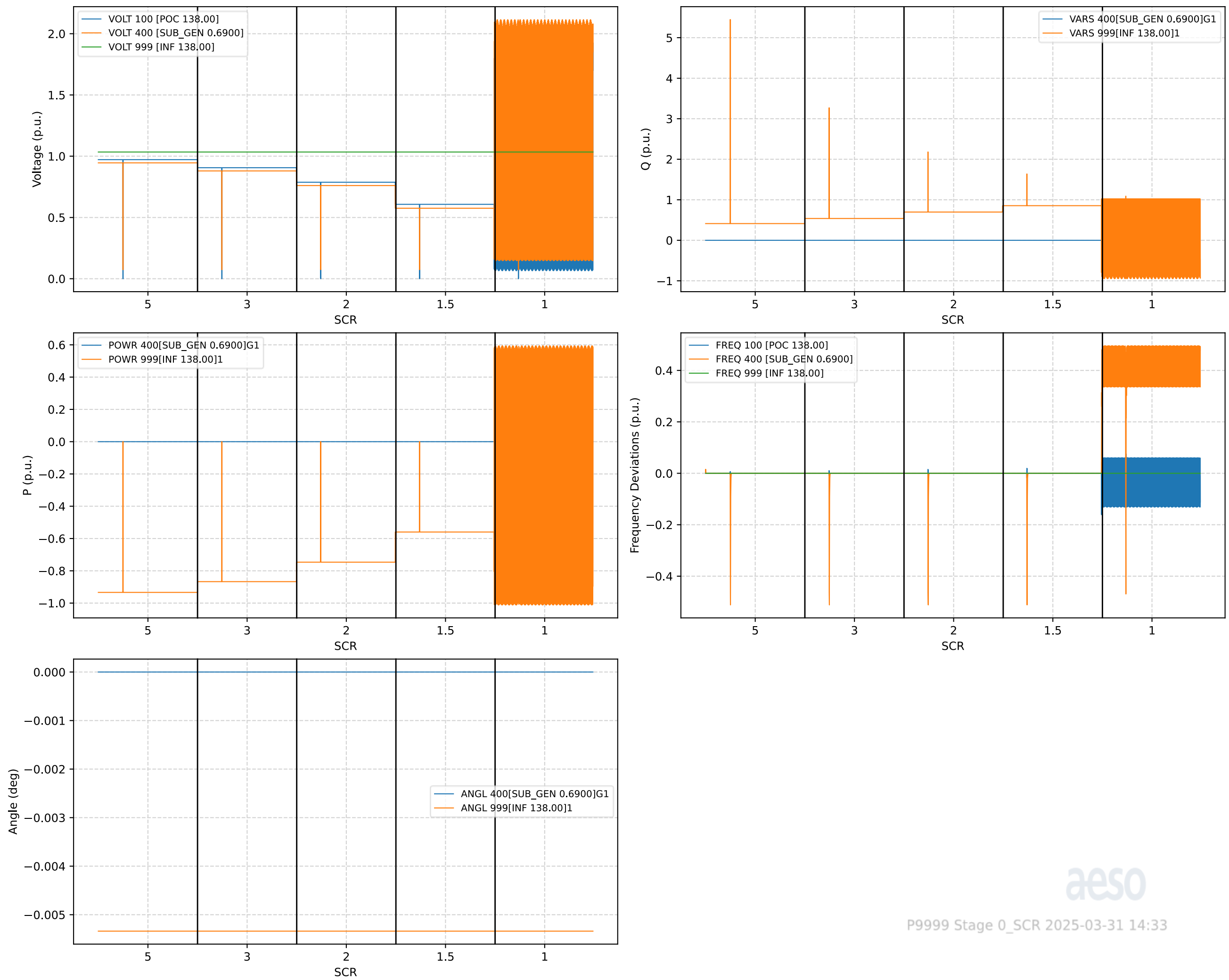

Figure 23 Sample SCR test results

7.12 Voltage reference step test

Under a +/-5% voltage reference step changes, the generator changes the reactive power output accordingly while real power is maintained.

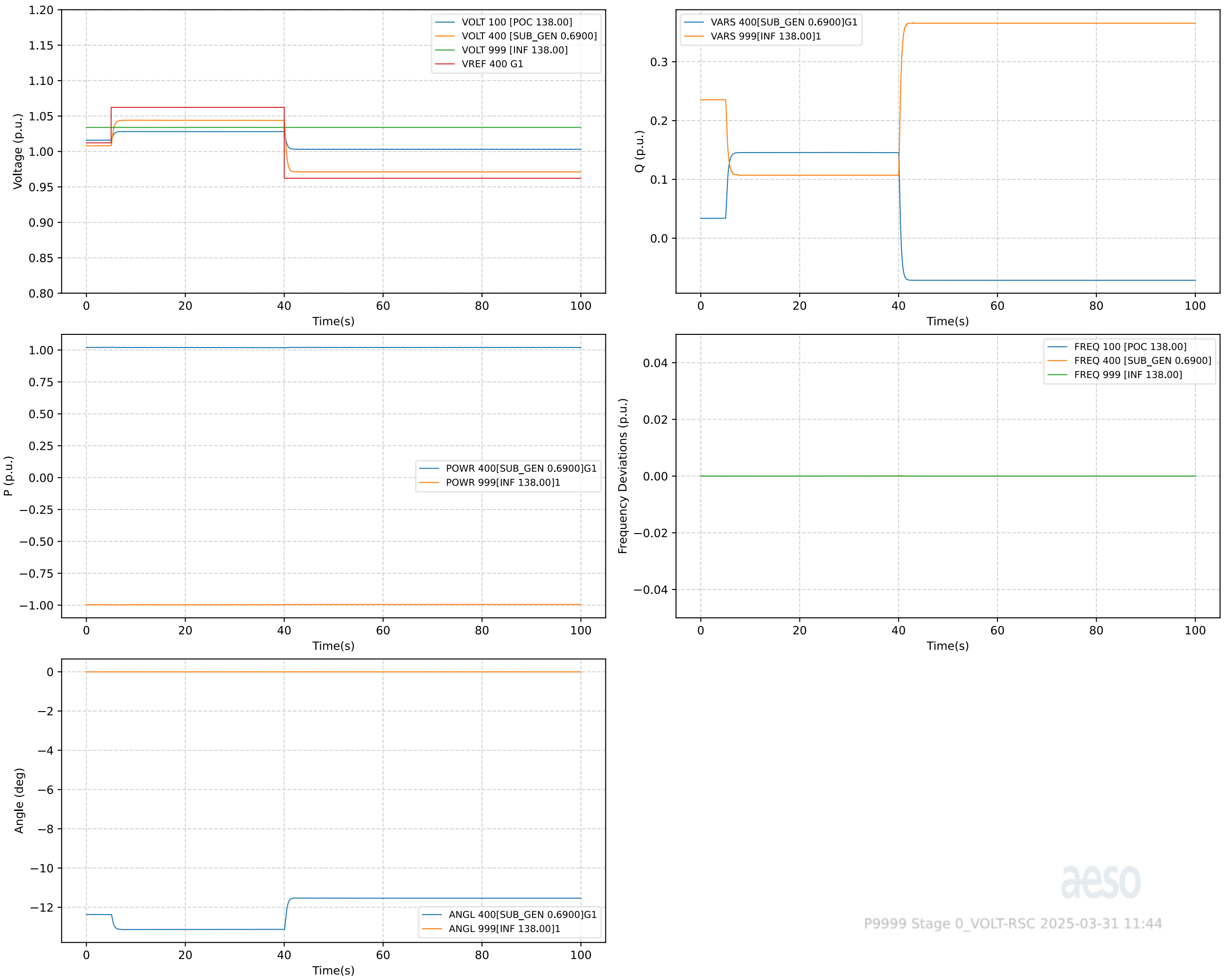

Figure 24 Sample voltage reference step test result

7.13 Frequency reference step test

In this test, real power is initialized at 80% of Pmax assumed in the power flow model. Under a +/-5% frequency reference step changes, the generator responds with active power changes accordingly. Since no headroom is reserved for underfrequency event, there is no change in active power during frequency reference step up.

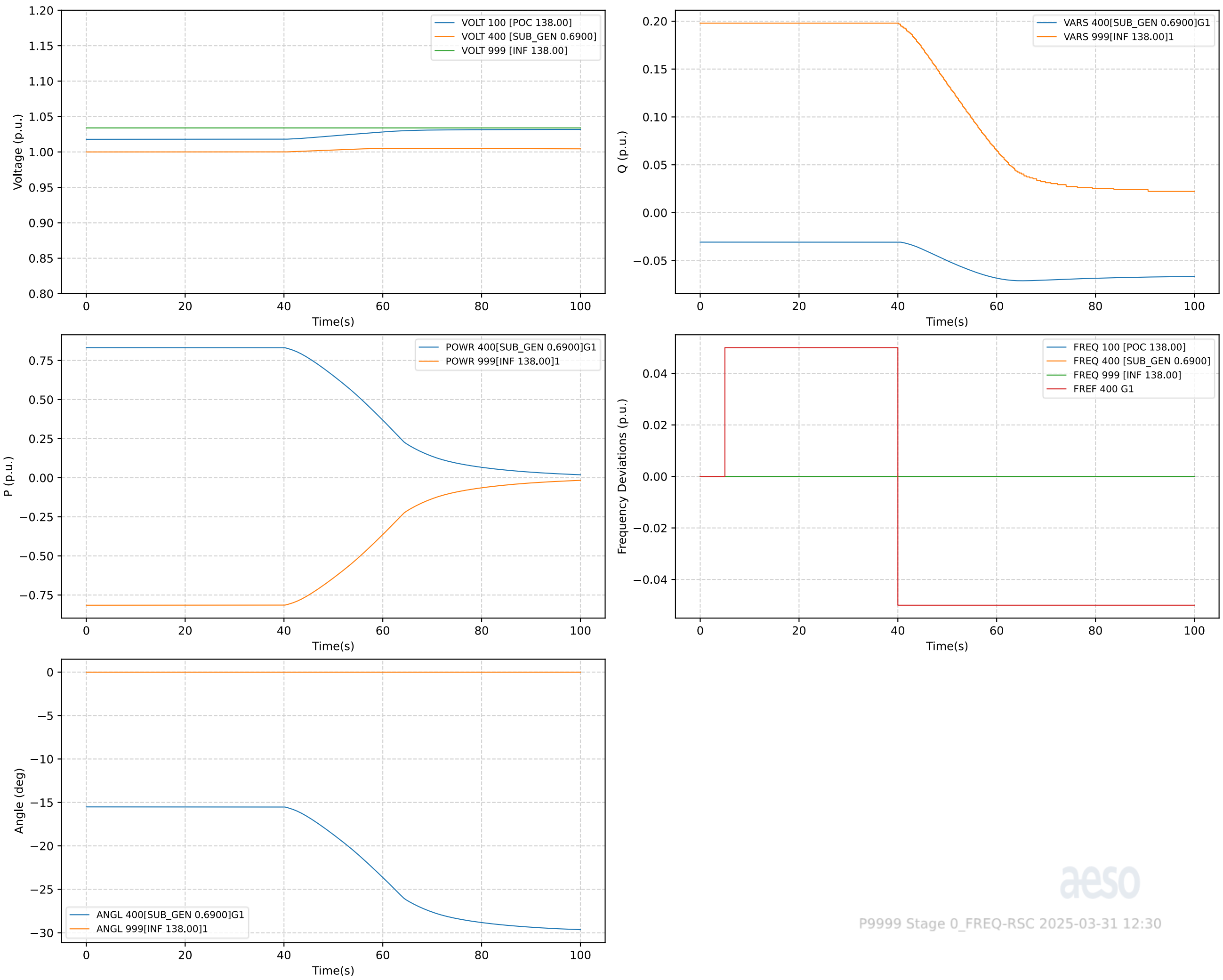

Figure 25 Sample frequency reference step test result